

DUAL HIGH-SPEED AUDIO OPERATIONAL AMPLIFIER

Check for Samples: [LM833](#)

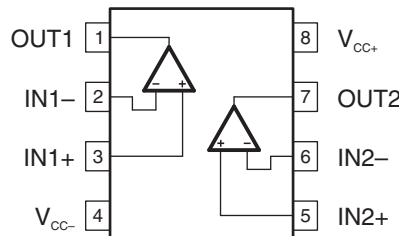
FEATURES

- **Dual-Supply Operation:** $\pm 5\text{ V}$ to $\pm 18\text{ V}$
- **Low Noise Voltage:** $4.5\text{ nV}/\sqrt{\text{Hz}}$
- **Low Input Offset Voltage:** 0.15 mV
- **Low Total Harmonic Distortion:** 0.002%
- **High Slew Rate:** $7\text{ V}/\mu\text{s}$
- **High-Gain Bandwidth Product:** 16 MHz
- **High Open-Loop AC Gain:** 800 at 20 kHz
- **Large Output-Voltage Swing:** 14.1 V to -14.6 V
- **Excellent Gain and Phase Margins**
- **Available in 8-Pin MSOP Package (3mm x 4.9mm x 0.65mm)**

APPLICATIONS

- **HiFi Audio System Equipment**
- **Preamplification and Filtering**
- **Set Top Box**
- **Microphone PreAmplifier Circuit**
- **General-Purpose Amplifier Applications**

D (SOIC), DGK (MSOP), OR P (PDIP) PACKAGE
(TOP VIEW)



DESCRIPTION

The LM833 is a dual operational amplifier with high-performance specifications for use in quality audio and data-signal applications. This device operates over a wide range of single- and dual-supply voltage with low noise, high-gain bandwidth, and high slew rate. Additional features include low total harmonic distortion, excellent phase and gain margins, large output voltage swing with no deadband crossover distortions, and symmetrical sink/source performance.

The dual amplifiers are utilized widely in circuit of audio optimized for all preamp and high level stages in PCM and HiFi systems. LM833 is pin-for-pin compatible with industry-standard dual operation amplifiers' pin assignments. With addition of a preamplifier, the gain of the power stage can be greatly reduced to improve performance.



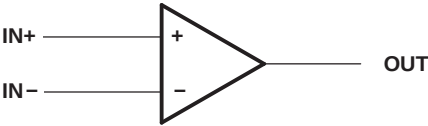
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION⁽¹⁾

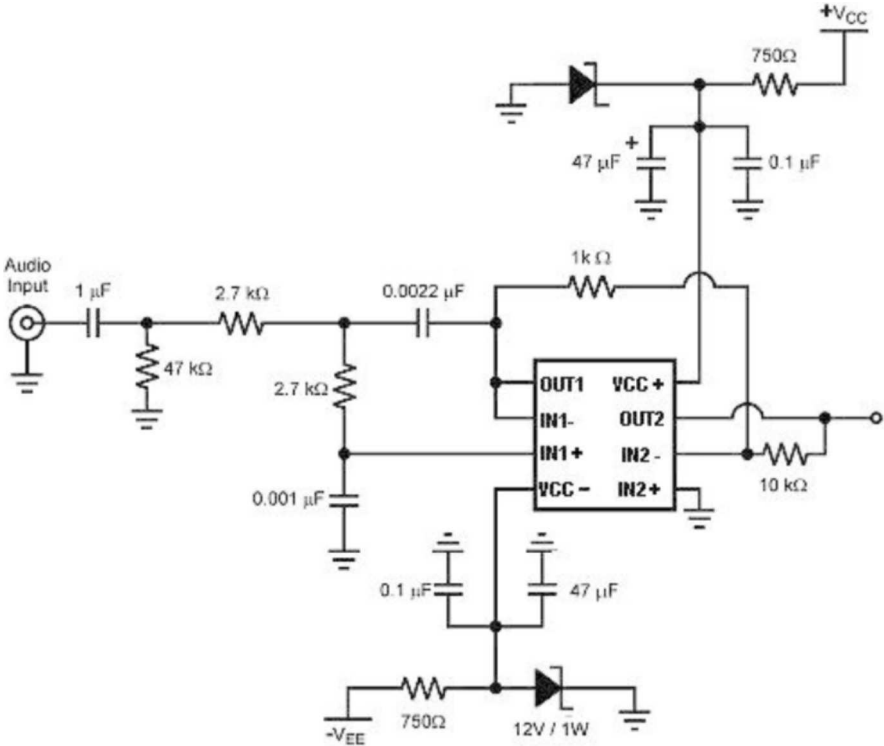
T _A	PACKAGE ⁽²⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽³⁾
–40°C to 85°C	PDIP – P	Tube of 50	LM833P	LM833P
	SOIC – D	Tube of 75	LM833D	LM833
		Reel of 2500	LM833DR	
	VSSOP/MSOP – DGK	Reel of 2500	LM833DGKR	RS_
		Reel of 250	LM833DGKT	

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) DGK: The actual top-side marking has one additional character that designates the wafer fab/assembly site.

Symbol (Each Amplifier)



Typical Design Example Audio Pre-Amplifier



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC+}	Supply voltage ⁽²⁾		18	V
V_{CC-}	Supply voltage ⁽²⁾		–18	V
$V_{CC+} - V_{CC-}$	Supply voltage		36	V
	Input voltage, either input ^{(2) (3)}		V_{CC+} or V_{CC-}	V
	Input current ⁽⁴⁾		±10	mA
	Duration of output short circuit ⁽⁵⁾		Unlimited	
θ_{JA}	Package thermal impedance, junction to free air ^{(6) (7)}	D package	97	°C/W
		DGK package	172	
		P package	85	
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-} .
- (3) The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
- (4) Excessive input current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs, unless some limiting resistance is used.
- (5) The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.
- (6) Maximum power dissipation is a function of $T_J(\text{max})$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (7) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTROSTATIC DISCHARGE RATINGS

		MIN	MAX	UNIT
ESD	Human-Body Model (HBM)		2.5	kV
	Charged-Device Model (CDM)		1.5	

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{CC-}	Supply voltage	–5	–18	V
V_{CC+}		5	18	
T_A	Operating free-air temperature range	–40	85	°C

ELECTRICAL CHARACTERISTICS

$V_{CC-} = -15\text{ V}$, $V_{CC+} = 15\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

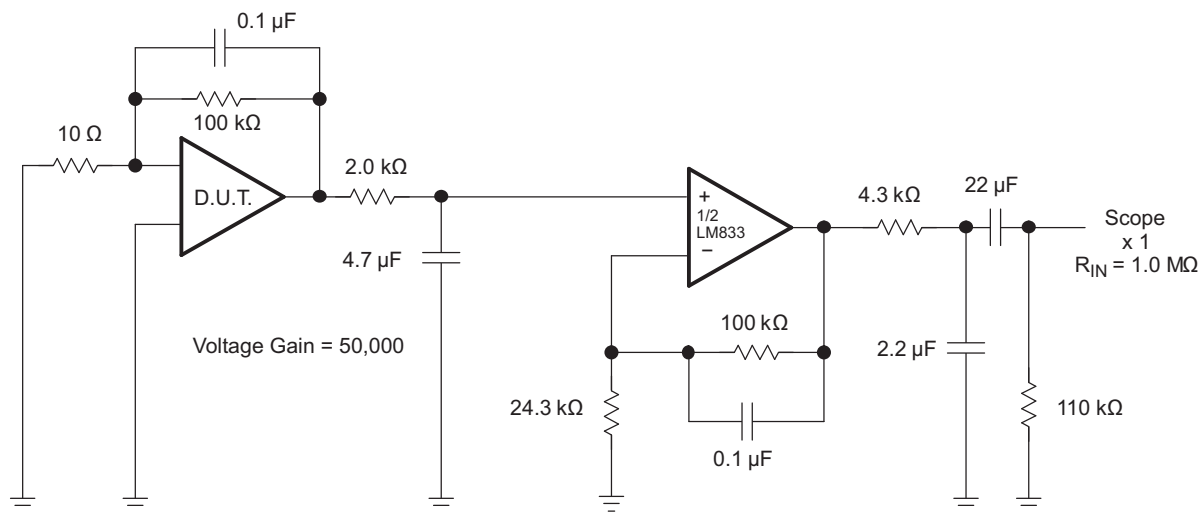
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V _{IO}	Input offset voltage	V _O = 0, R _S = 10 Ω, V _{CM} = 0	T _A = 25°C	0.15	2	mV	
			T _A = −40°C to 85°C		3		
αV _{IO}	Input offset voltage temperature coefficient	V _O = 0, R _S = 10 Ω, V _{CM} = 0	T _A = −40°C to 85°C	2		μV/°C	
I _{IB}	Input bias current	V _O = 0, V _{CM} = 0	T _A = 25°C	300	750	nA	
			T _A = −40°C to 85°C		800		
I _{IO}	Input offset current	V _O = 0, V _{CM} = 0	T _A = 25°C	25	150	nA	
			T _A = −40°C to 85°C		175		
V _{ICR}	Common-mode input voltage range	ΔV _{IO} = 5 mV, V _O = 0		±13	±14	V	
A _{VD}	Large-signal differential voltage amplification	R _L ≥ 2 kΩ, V _O = ±10 V	T _A = 25°C	90	110	dB	
			T _A = −40°C to 85°C	85			
V _{OM}	Maximum output voltage swing	V _{ID} = ±1 V	R _L = 600 Ω	V _{OM+}	10.7	V	
				V _{OM−}	−11.9		
			R _L = 2k Ω	V _{OM+}	13.2		13.8
				V _{OM−}	−13.2		−13.7
			R _L = 10k Ω	V _{OM+}	13.5		14.1
				V _{OM−}	−14		−14.6
CMMR	Common-mode rejection ratio	V _{IN} = ±13 V		80	100	dB	
k _{SVR} ⁽¹⁾	Supply-voltage rejection ratio	V _{CC+} = 5 V to 15 V, V _{CC−} = −5 V to −15 V		80	105	dB	
I _{OS}	Output short-circuit current	V _{ID} = 1 V, Output to GND	Source current	15	29	mA	
			Sink current	−20	−37		
I _{CC}	Supply current (per channel)	V _O = 0	T _A = 25°C	2.05	2.5	mA	
			T _A = −40°C to 85°C		2.75		

(1) Measured with $V_{CC\pm}$ differentially varied at the same time

OPERATING CHARACTERISTICS

$V_{CC-} = -15\text{ V}$, $V_{CC+} = 15\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$A_{VD} = 1$, $V_{IN} = -10\text{ V}$ to 10 V , $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$		5	7		V/ μs
GBW	Gain bandwidth product	$f = 100\text{ kHz}$		10	16		MHz
B_1	Unity gain frequency	Open loop			9		MHz
G_m	Gain margin	$R_L = 2\text{ k}\Omega$	$C_L = 0\text{ pF}$		-11		dB
			$C_L = 100\text{ pF}$		-6		
Φ_m	Phase margin	$R_L = 2\text{ k}\Omega$	$C_L = 0\text{ pF}$		55		deg
			$C_L = 100\text{ pF}$		40		
	Amp-to-amp isolation	$f = 20\text{ Hz}$ to 20 kHz			-120		dB
	Power bandwidth	$V_O = 27\text{ V}_{(PP)}$, $R_L = 2\text{ k}\Omega$, THD $\leq 1\%$			120		kHz
THD	Total harmonic distortion	$V_O = 3\text{ V}_{rms}$, $A_{VD} = 1$, $R_L = 2\text{ k}\Omega$, $f = 20\text{ Hz}$ to 20 kHz			0.002		%
z_o	Open-loop output impedance	$V_O = 0$, $f = 9\text{ MHz}$			37		Ω
r_{id}	Differential input resistance	$V_{CM} = 0$			175		k Ω
C_{id}	Differential input capacitance	$V_{CM} = 0$			12		pF
V_n	Equivalent input noise voltage	$f = 1\text{ kHz}$, $R_S = 100\ \Omega$			4.5		nV/ $\sqrt{\text{Hz}}$
I_n	Equivalent input noise current	$f = 1\text{ kHz}$			0.5		pA/ $\sqrt{\text{Hz}}$

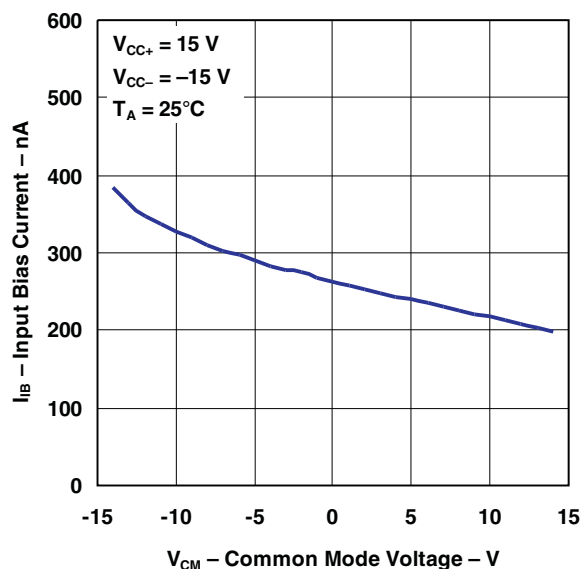


NOTE: All capacitors are non-polarized.

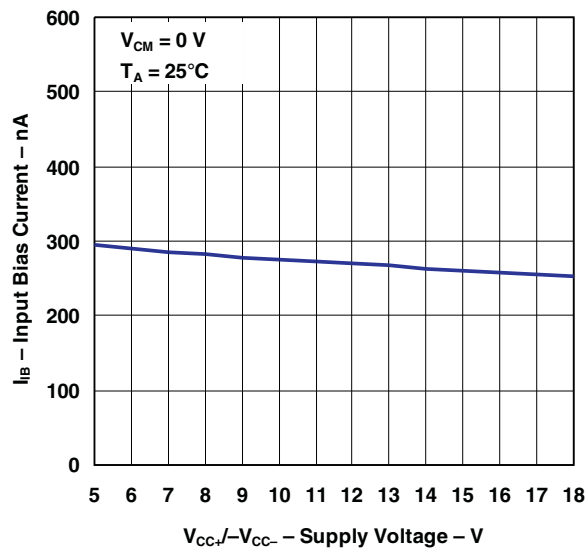
Figure 1. Voltage Noise Test Circuit (0.1 Hz to 10 Hz)

TYPICAL CHARACTERISTICS

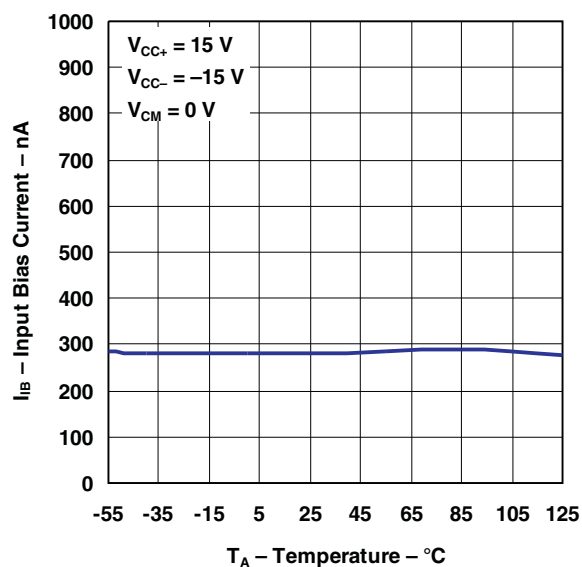
INPUT BIAS CURRENT
vs
COMMON-MODE VOLTAGE



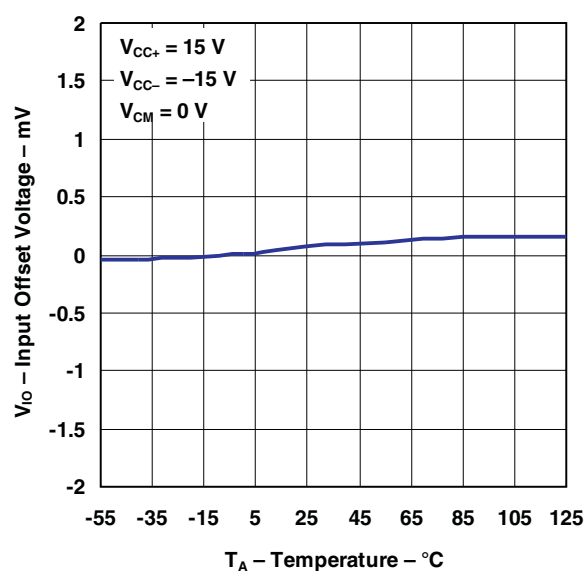
INPUT BIAS CURRENT
vs
SUPPLY VOLTAGE



INPUT BIAS CURRENT
vs
TEMPERATURE

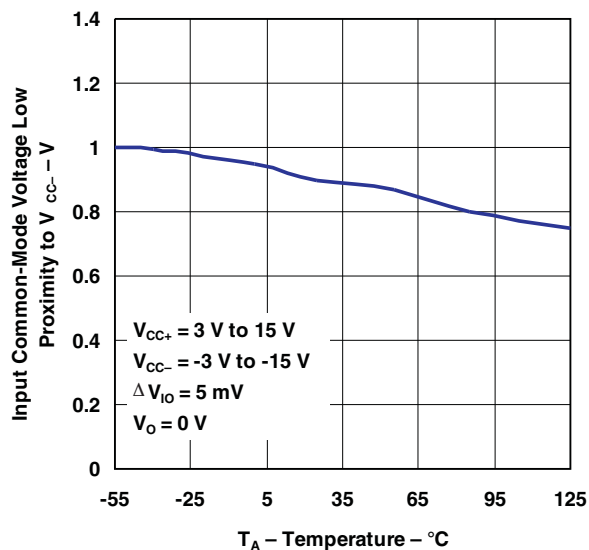


INPUT OFFSET VOLTAGE
vs
TEMPERATURE

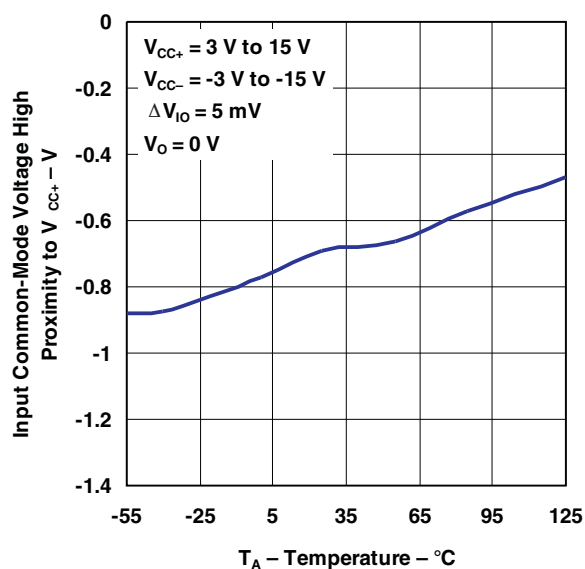


TYPICAL CHARACTERISTICS (continued)

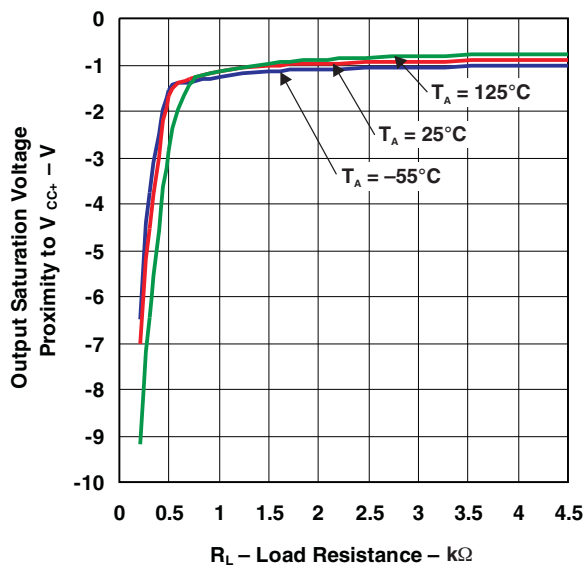
INPUT COMMON-MODE VOLTAGE
LOW PROXIMITY TO V_{CC-}
VS
TEMPERATURE



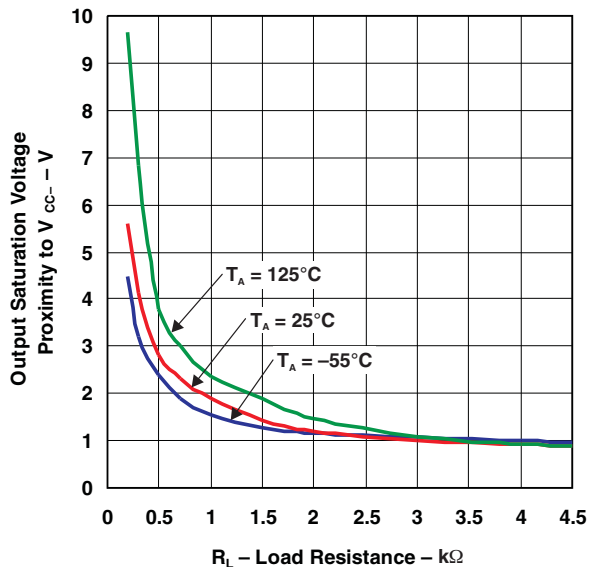
INPUT COMMON-MODE VOLTAGE
HIGH PROXIMITY TO V_{CC+}
VS
TEMPERATURE



OUTPUT SATURATION VOLTAGE PROXIMITY TO V_{CC+}
VS
LOAD RESISTANCE

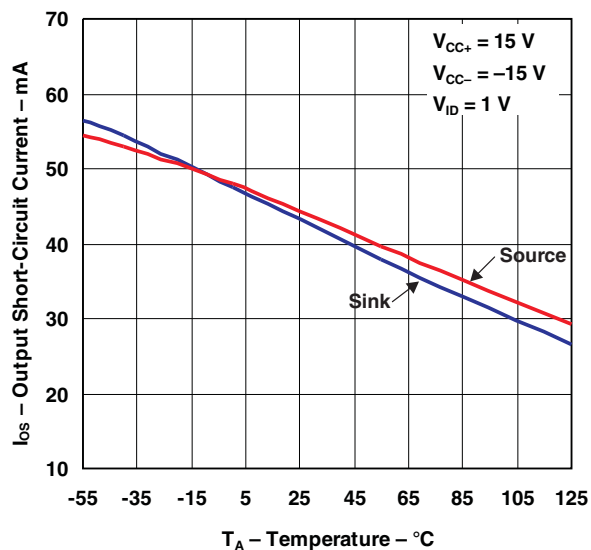


OUTPUT SATURATION VOLTAGE PROXIMITY TO V_{CC-}
VS
LOAD RESISTANCE

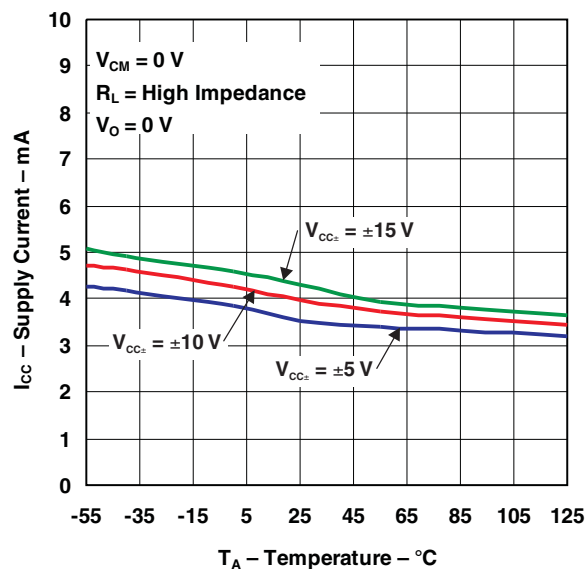


TYPICAL CHARACTERISTICS (continued)

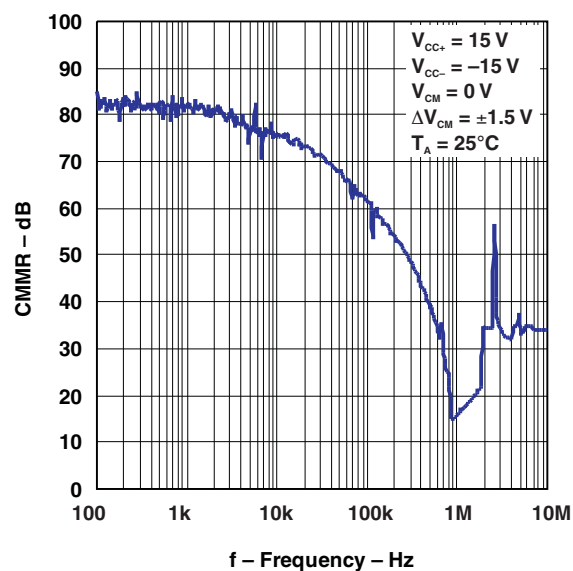
OUTPUT SHORT-CIRCUIT CURRENT
VS
TEMPERATURE



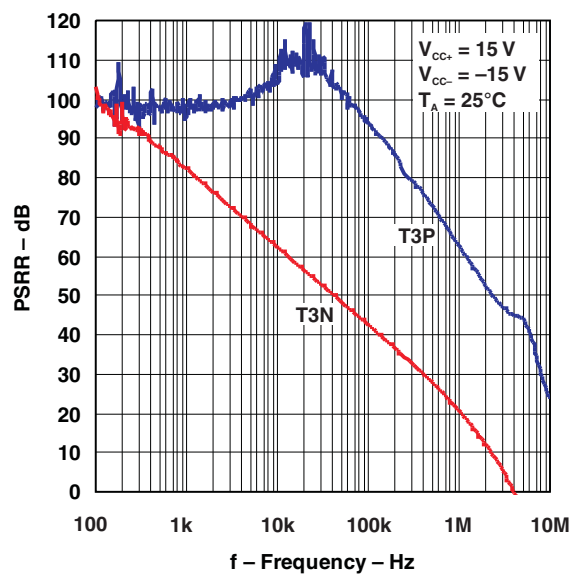
SUPPLY CURRENT
VS
TEMPERATURE



CMRR
VS
FREQUENCY

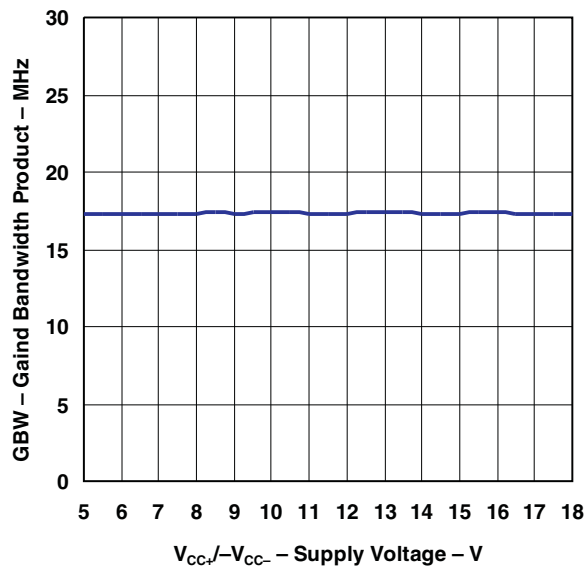


PSSR
VS
FREQUENCY

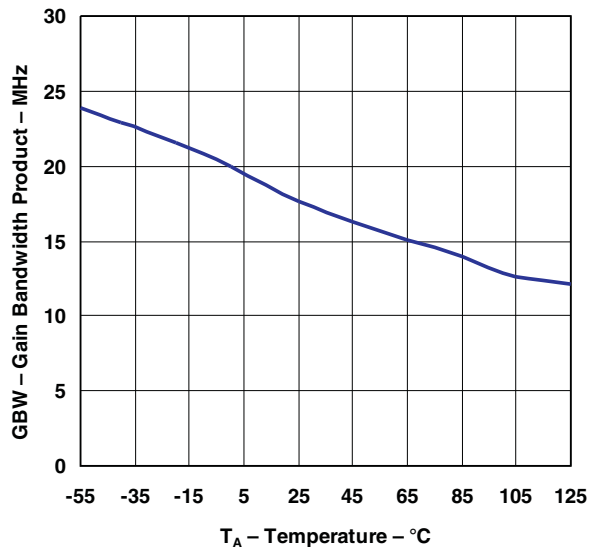


TYPICAL CHARACTERISTICS (continued)

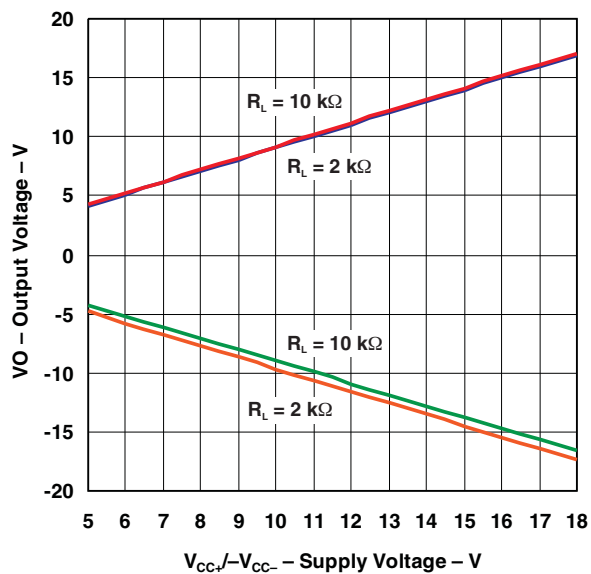
GAIN BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE



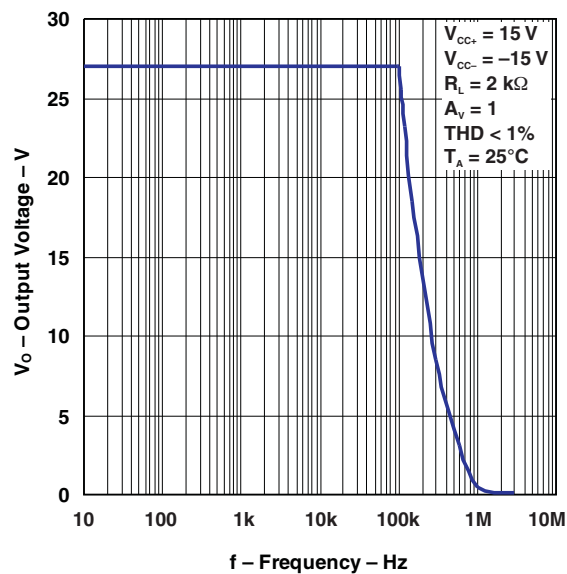
GAIN BANDWIDTH PRODUCT
vs
TEMPERATURE



OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

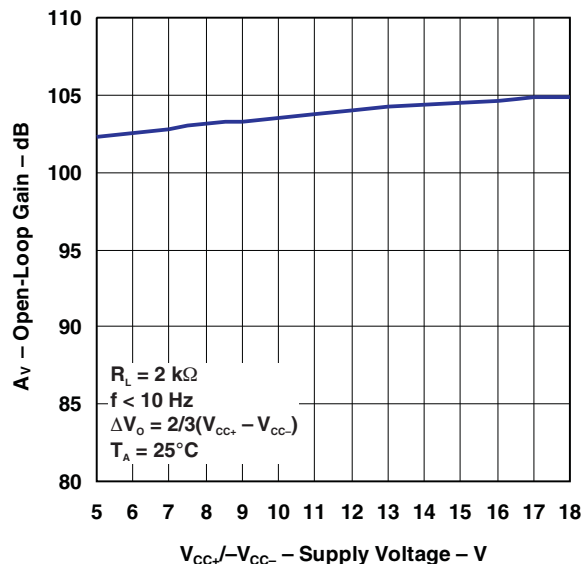


OUTPUT VOLTAGE
vs
FREQUENCY

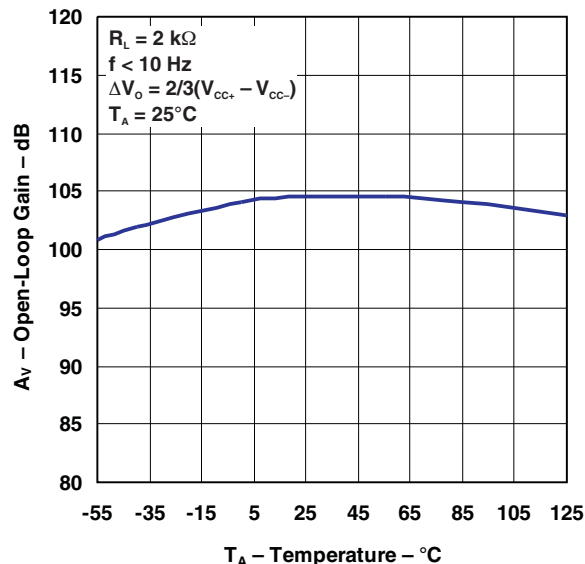


TYPICAL CHARACTERISTICS (continued)

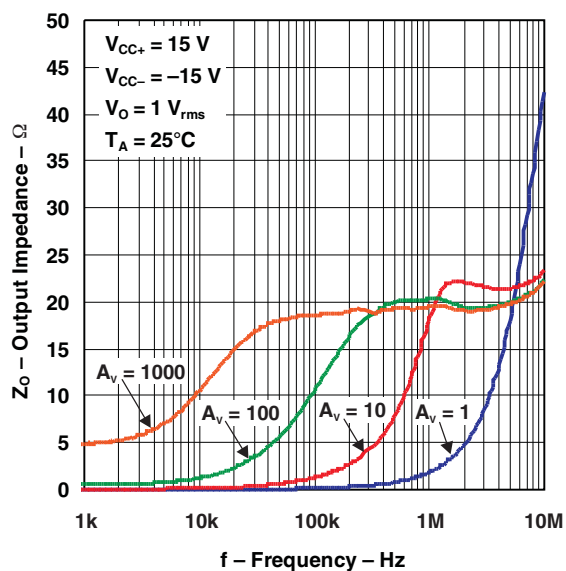
OPEN-LOOP GAIN
VS
SUPPLY VOLTAGE



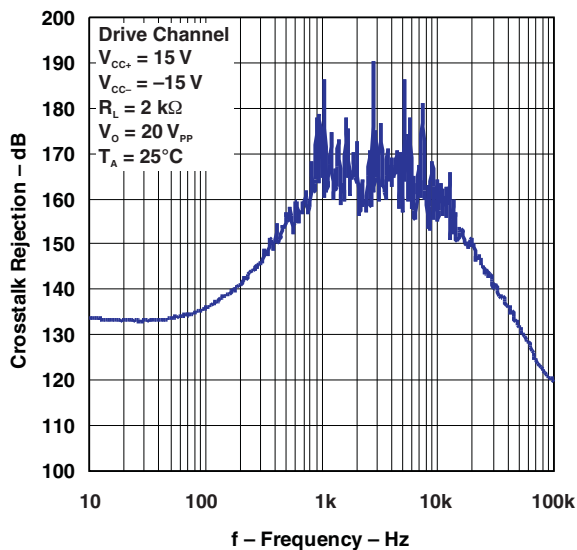
OPEN-LOOP GAIN
VS
TEMPERATURE



OUTPUT IMPEDANCE
VS
FREQUENCY

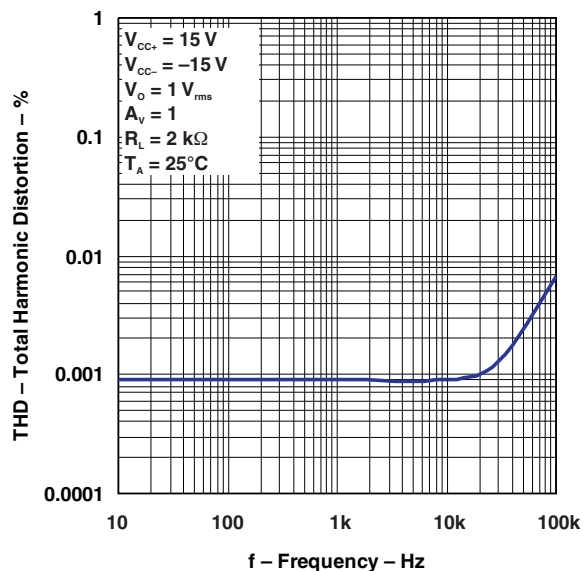


CROSSTALK REJECTION
VS
FREQUENCY

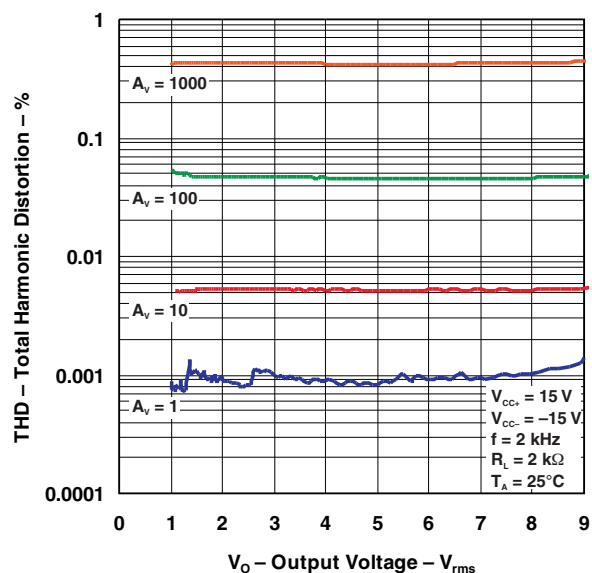


TYPICAL CHARACTERISTICS (continued)

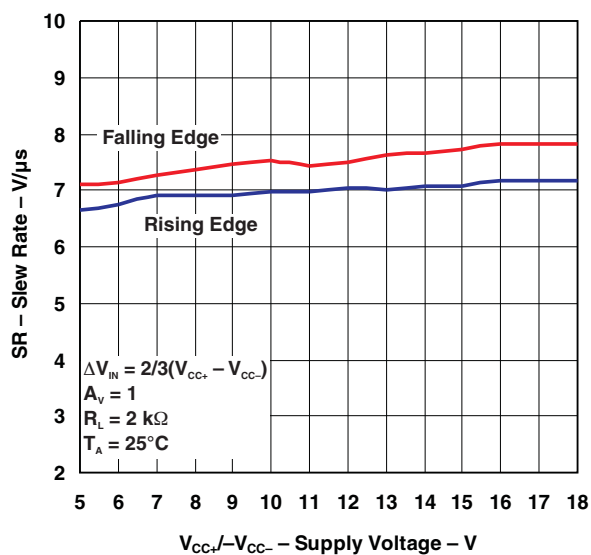
TOTAL HARMONIC DISTORTION
vs
FREQUENCY



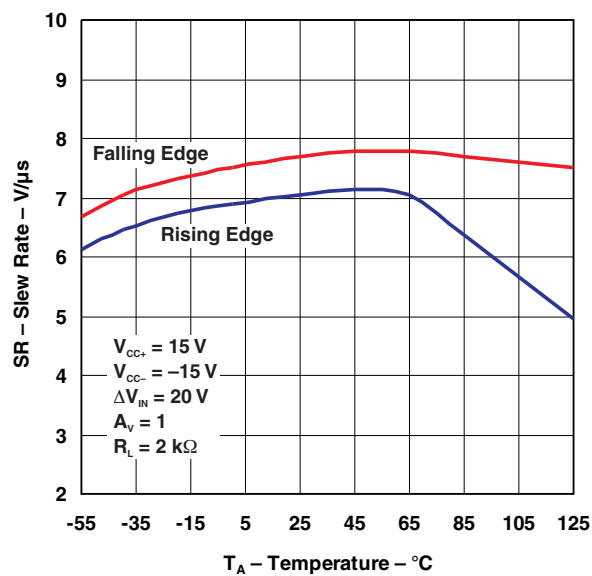
TOTAL HARMONIC DISTORTION
vs
OUTPUT VOLTAGE



SLEW RATE
vs
SUPPLY VOLTAGE

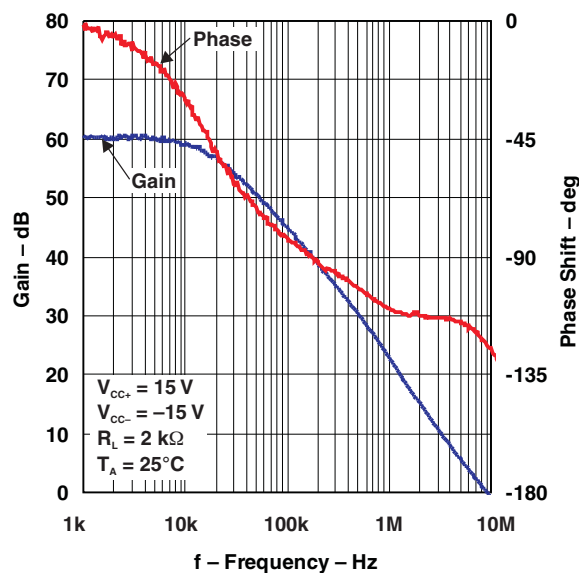


SLEW RATE
vs
TEMPERATURE

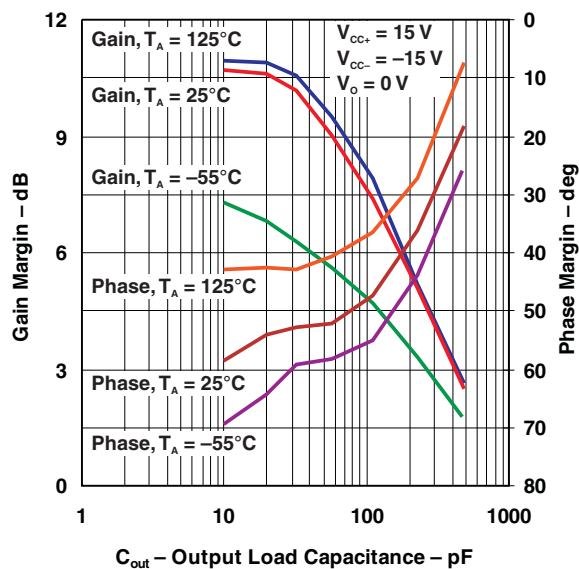


TYPICAL CHARACTERISTICS (continued)

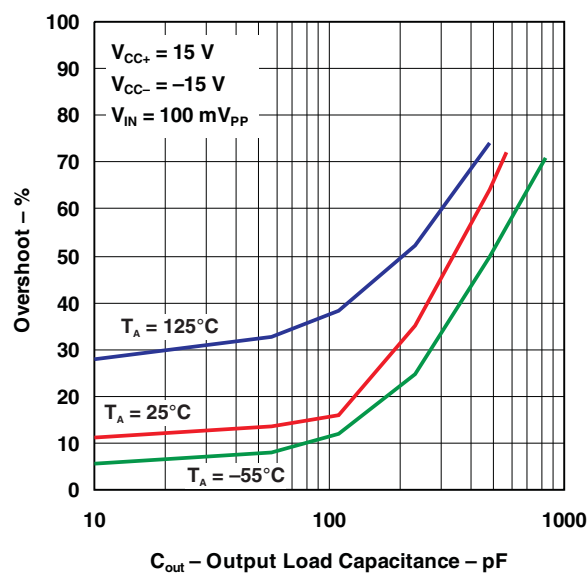
GAIN AND PHASE
VS
FREQUENCY



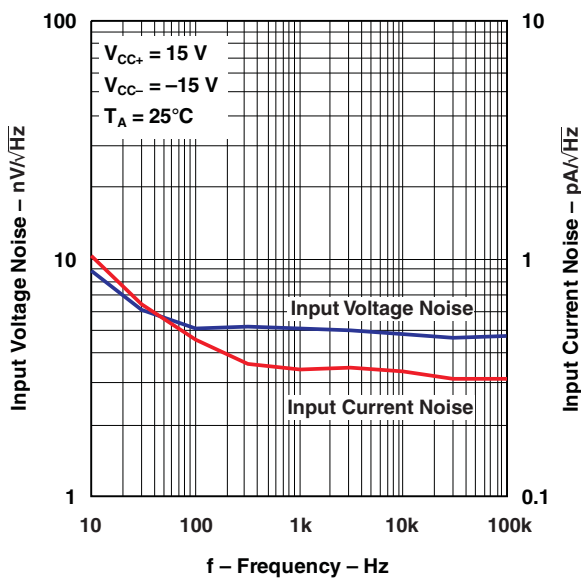
GAIN AND PHASE MARGIN
VS
OUTPUT LOAD CAPACITANCE



OVERSHOOT
VS
OUTPUT LOAD CAPACITANCE

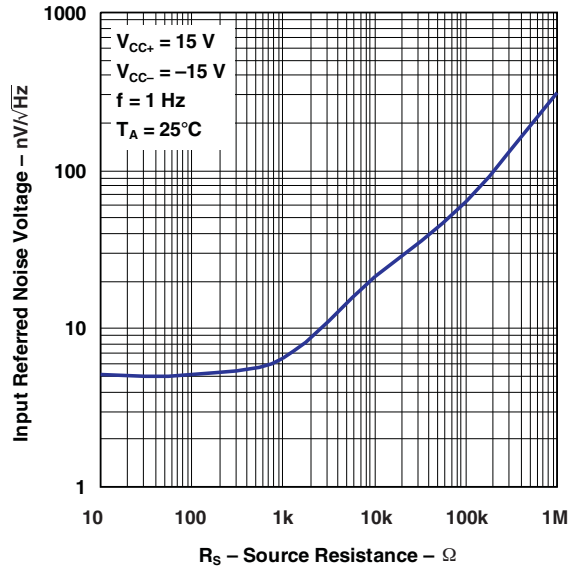


INPUT VOLTAGE AND CURRENT NOISE
VS
FREQUENCY

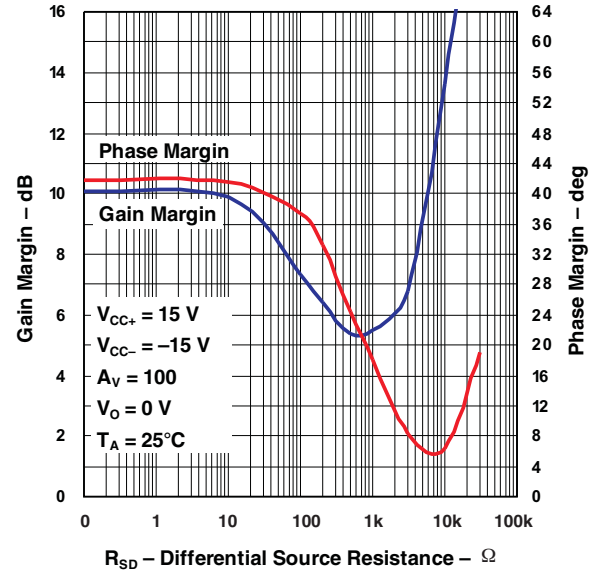


TYPICAL CHARACTERISTICS (continued)

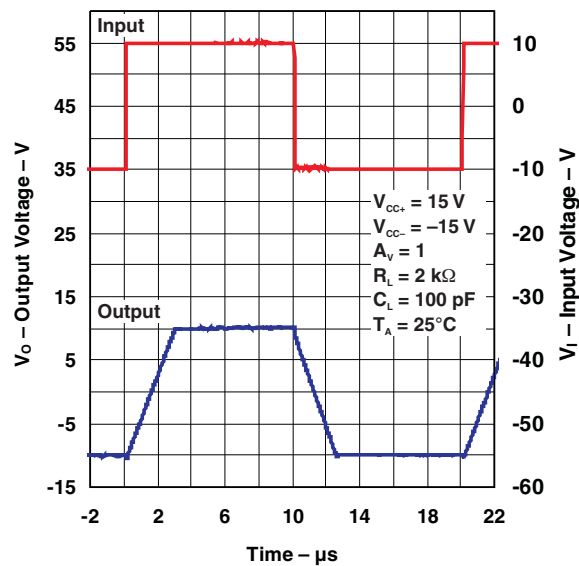
INPUT REFERRED NOISE VOLTAGE
VS
SOURCE RESISTANCE



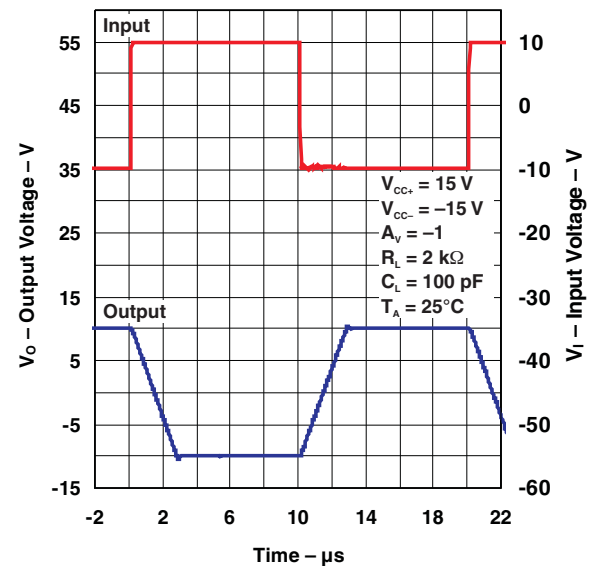
GAIN AND PHASE MARGIN
VS
DIFFERENTIAL SOURCE RESISTANCE



LARGE SIGNAL TRANSIENT RESPONSE
($A_V = 1$)

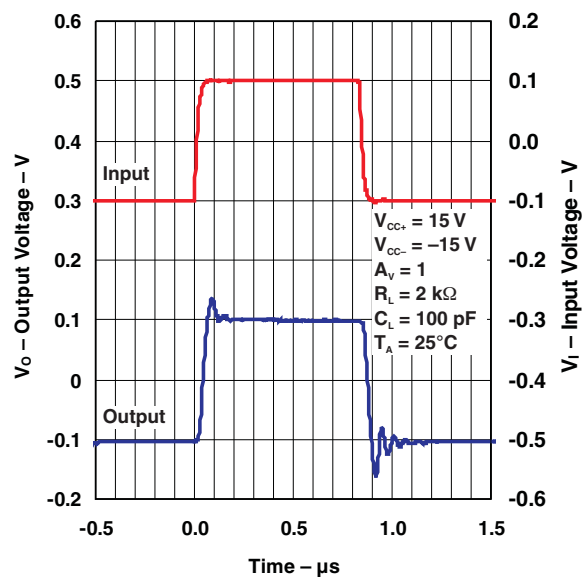


LARGE SIGNAL TRANSIENT RESPONSE
($A_V = -1$)

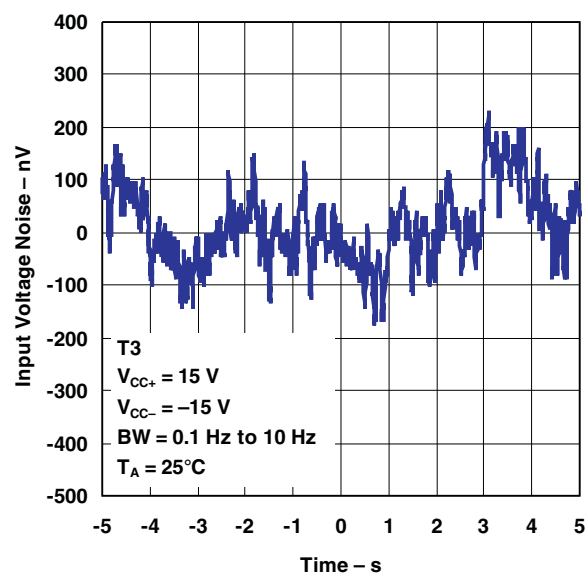


TYPICAL CHARACTERISTICS (continued)

SMALL SIGNAL TRANSIENT RESPONSE



LOW FREQUENCY NOISE

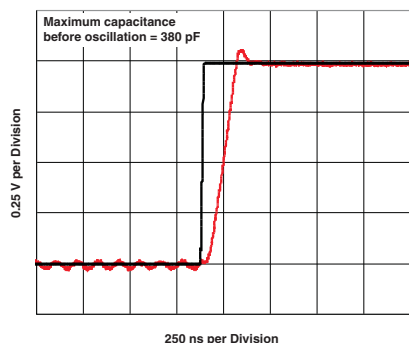


APPLICATION INFORMATION

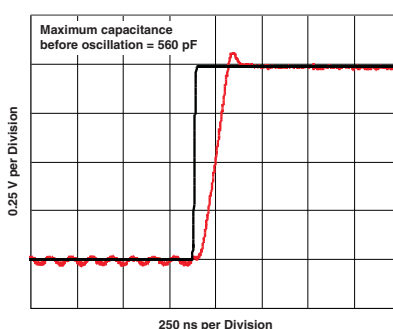
Output Characteristics

All operating characteristics are specified with 100-pF load capacitance. The LM833 can drive higher capacitance loads. However, as the load capacitance increases, the resulting response pole occurs at lower frequencies, causing ringing, peaking, or oscillation. The value of the load capacitance at which oscillation occurs varies from lot to lot. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem (see Figure 2).

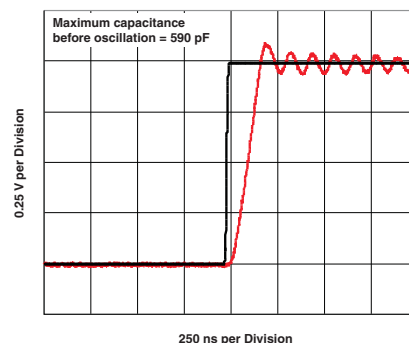
PULSE RESPONSE
($R_L = 600\ \Omega$, $C_L = 380\ \text{pF}$)



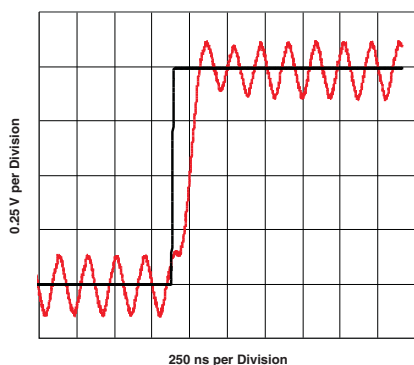
PULSE RESPONSE
($R_L = 2\ \text{k}\Omega$, $C_L = 560\ \text{pF}$)



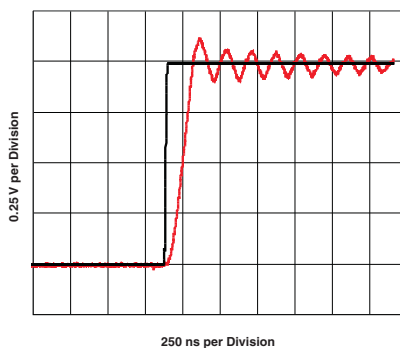
PULSE RESPONSE
($R_L = 10\ \text{k}\Omega$, $C_L = 590\ \text{pF}$)



PULSE RESPONSE
($R_O = 0\ \Omega$, $C_O = 1000\ \text{pF}$, $R_L = 2\ \text{k}\Omega$)



PULSE RESPONSE
($R_O = 4\ \Omega$, $C_O = 1000\ \text{pF}$, $R_L = 2\ \text{k}\Omega$)



PULSE RESPONSE
($R_O = 35\ \Omega$, $C_O = 1000\ \text{pF}$, $R_L = 2\ \text{k}\Omega$)

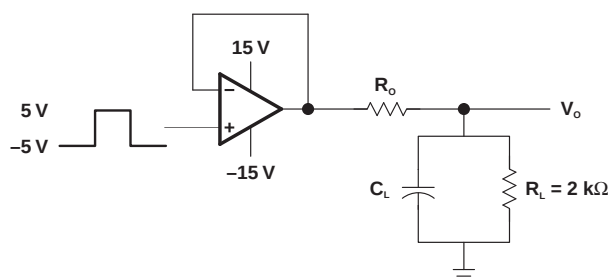
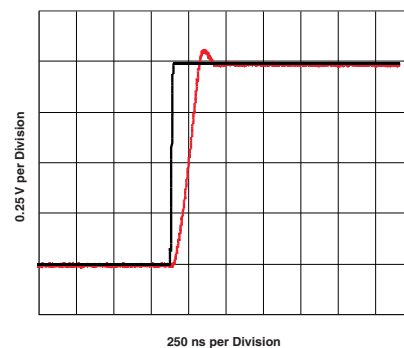


Figure 2. Output Characteristics

REVISION HISTORY

Changes from Original (July 2010) to Revision A	Page
• Changed Datasheet status from Product Preview to Production Data.	1

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
LM833D	ACTIVE	SOIC	D	8	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LM833DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LM833DGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LM833DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
LM833P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

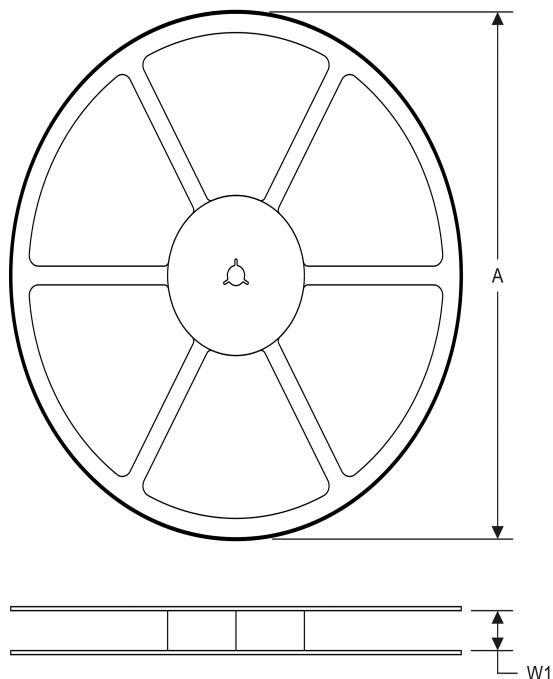
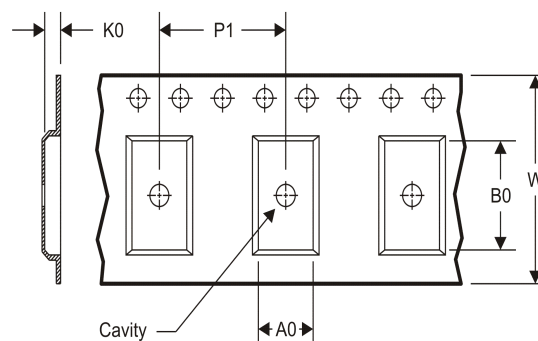
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


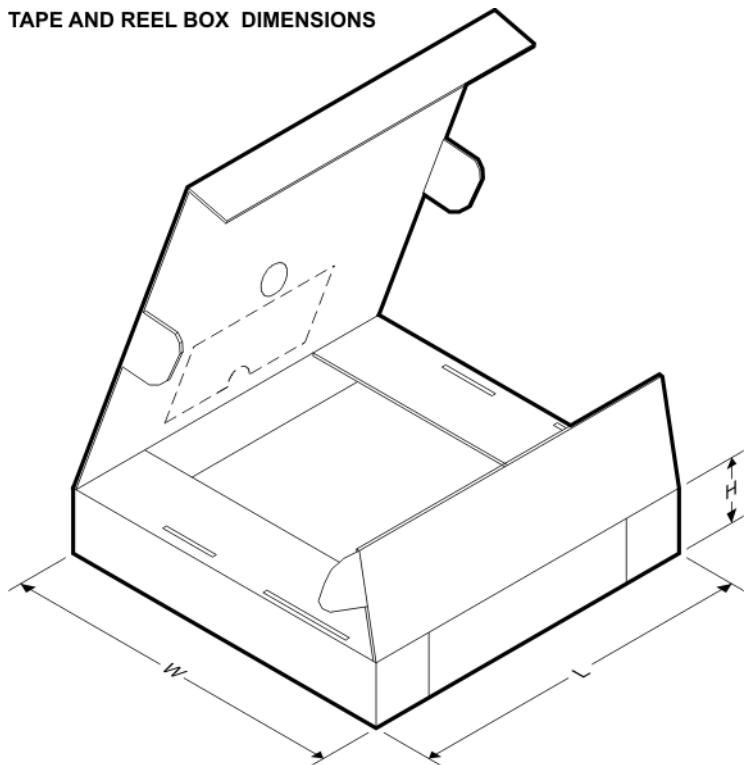
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM833DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
LM833DGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
LM833DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM833DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

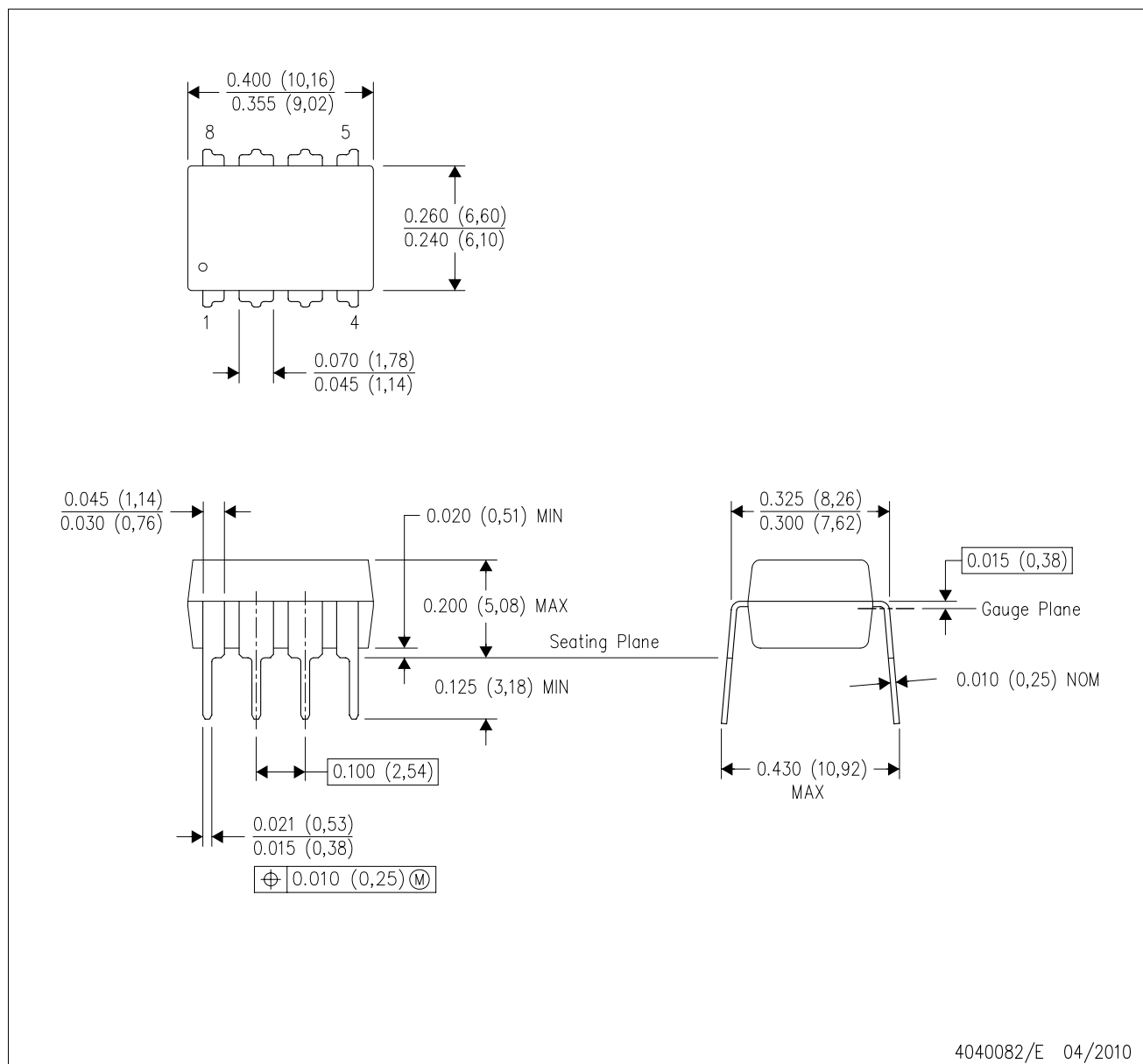


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM833DGKR	VSSOP	DGK	8	2500	346.0	346.0	35.0
LM833DGKT	VSSOP	DGK	8	250	203.0	203.0	35.0
LM833DR	SOIC	D	8	2500	367.0	367.0	35.0
LM833DR	SOIC	D	8	2500	340.5	338.1	20.6

P (R-PDIP-T8)

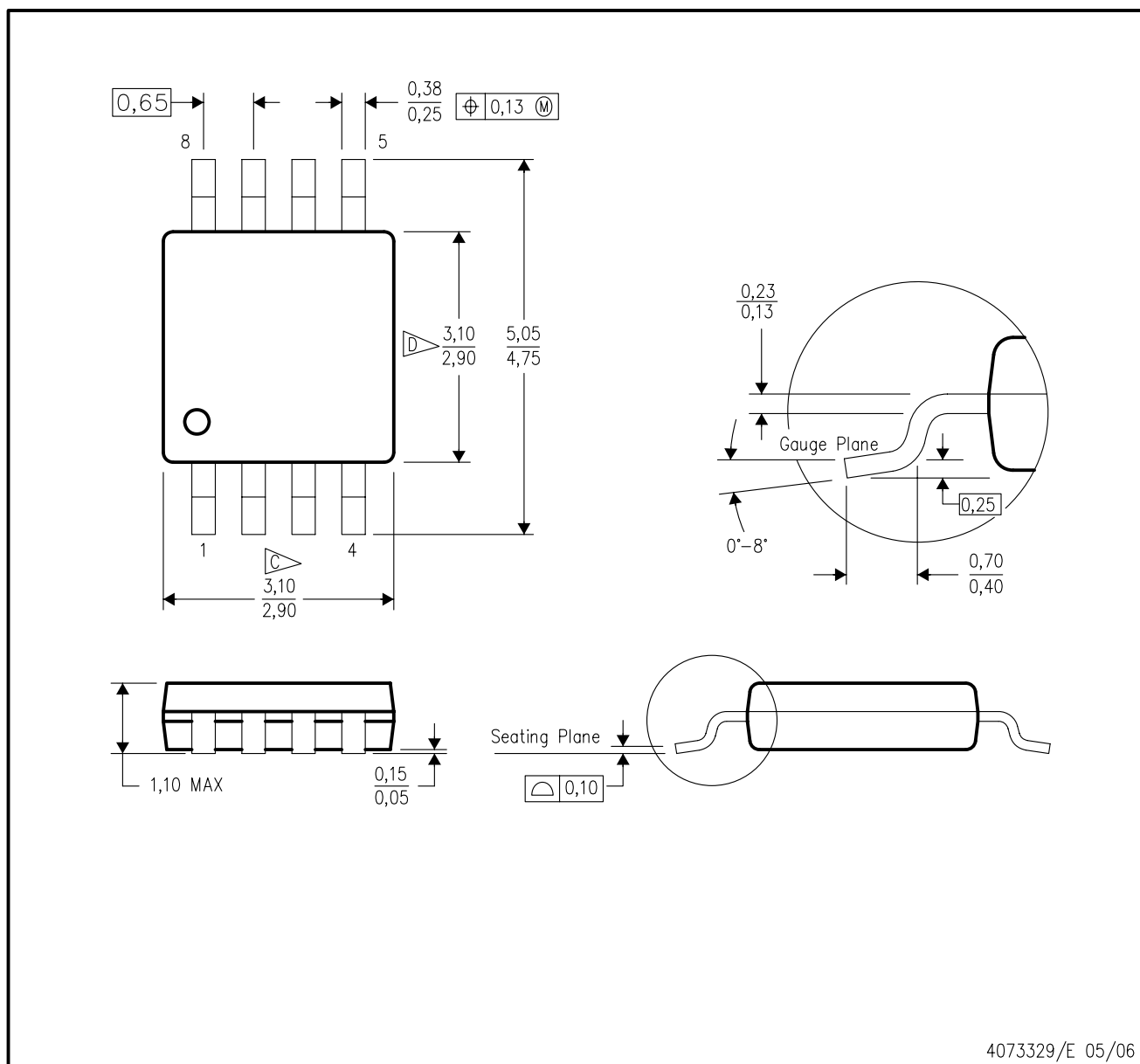
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

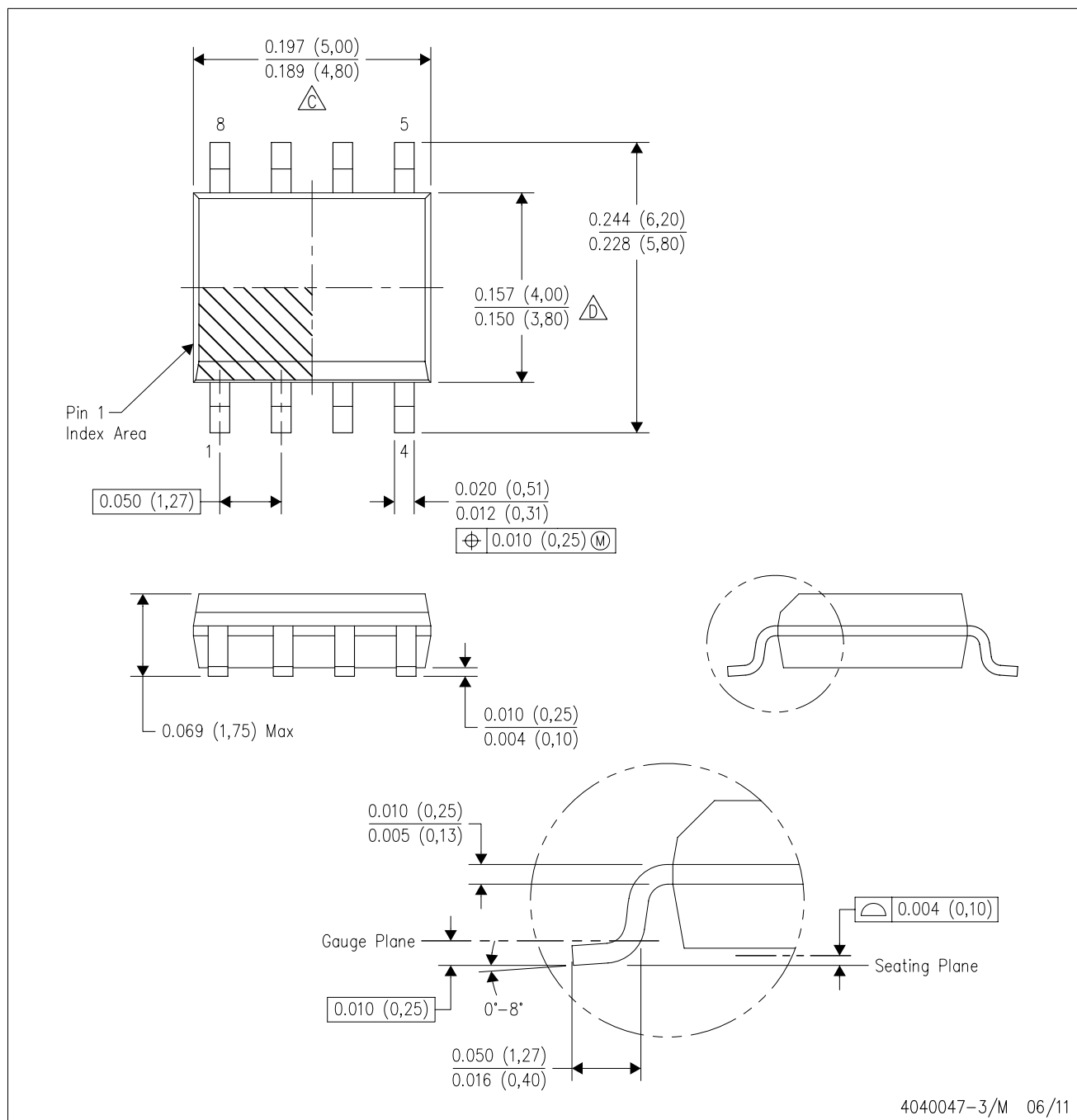


NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R-PDSO-G8)

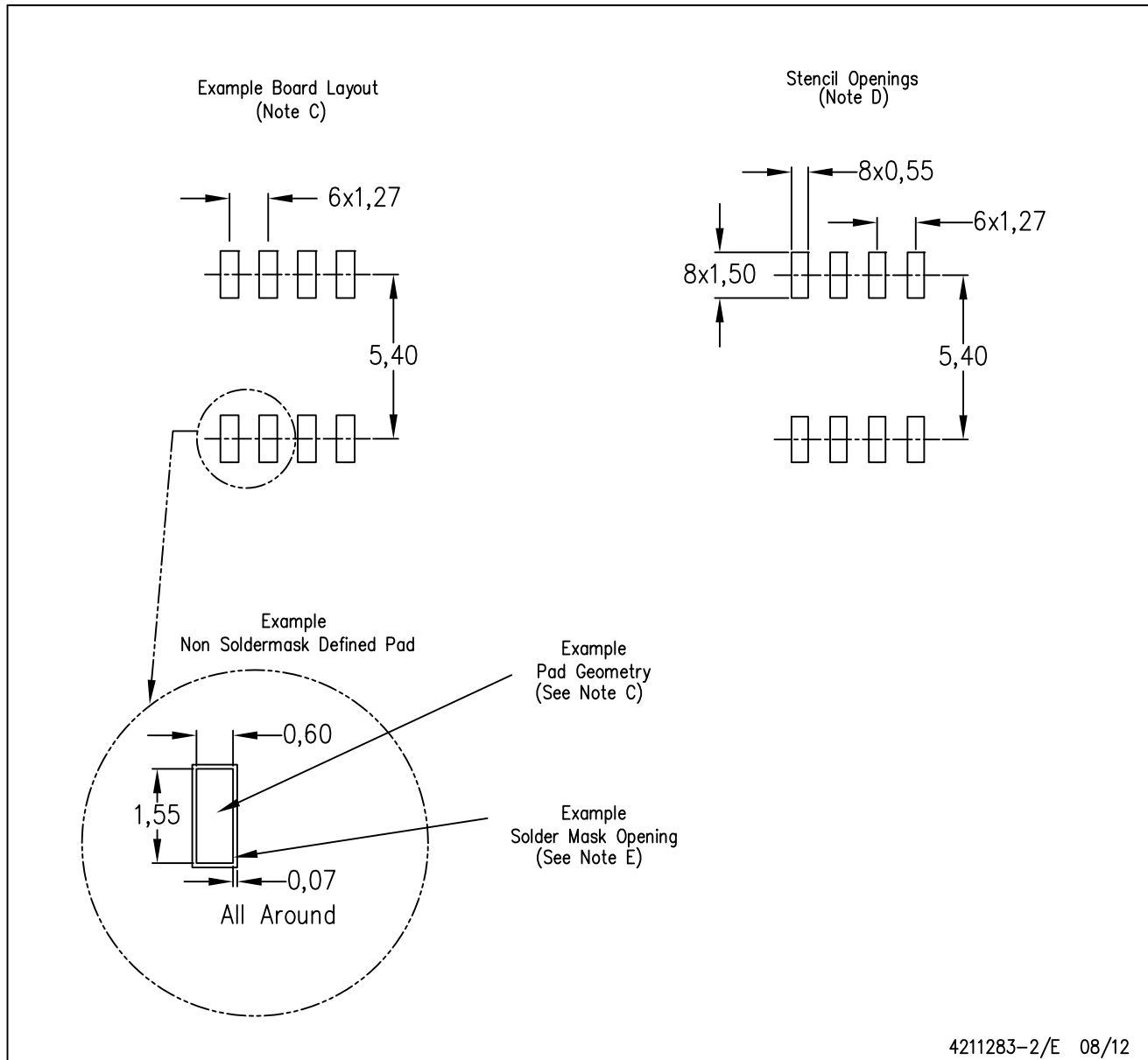
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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