4. AF Circuits

4.1 Hi-Fi AF output stages using SIPMOS transistors

Recently, increasing attention is payed to MOSFET hi-fi power output stages. Because of the wide power bandwidth, highly insignificant distortion, and high output power, they are setting new standards in amplifier technology.

Figure 4.1 shows a SIPMOS output stage featuring an output power between 60 W and 160 W. The circuit is based on a drive circuit, specially developed for SIPMOS transistors, that can easily be adapted to various requirements such as performance, bandwidth, and distortion. The circuit can also be used as a power op amp, for example in control systems, where such amplifiers are increasingly required.

The electrical data of the output stage surpasses the hi-fi standard DIN 45500 in all values. These output stages show very good characteristics in comparison with high quality bipolar or other MOSFET hi-fi amplifiers. They are short-circuit proof and protected against excess temperature.

SIPMOS transistors are voltage-controlled. The input resistance is approx. $10^9\ \Omega$ and parallel to this is 0.1 nF to 1.2 nF of capacitance. Thus, the control power for audio frequencies is comparatively low. When selecting the drive circuit, conventional circuit principles of bipolar amplifier technology could not be applied because only N channel SIPMOS transistors are available, and because a quasi-complementary circuit, using bipolar and SIPMOS transistors, would be unfavorable for its high dissymmetries. Also, the high quality requirements imposed upon the output stage presupposes circuit symmetry. Therefore, new ways had to be discovered.

Two series-connected SIPMOS transistors are driven by a two-output differential amplifier. The output currents of the differential amplifier have a phase displacement of 180°. This current through the load resistor, which is connected in parallel to the source-gate, generates the respective gate-source voltage as drive signal for the SIPMOS transistors. The output of the final stage is dc-coupled with negative feedback to the inverting input of the differential amplifier through the resistor R = 33 kΩ and ac-coupled by means of an *RC* network 1 kΩ/100 µF.

The high open-loop gain keeps the average voltage at the output of the final stage constant and – by negative feedback – forces a high linearity and thereby a low distortion. The transmission characteristic I_D (V_{GS}) which in case of an AB amplifier is non-linear, has almost no effect on the amplifier characteristics.

The output power of the output stage can easily be increased by simply paralleling[1]) additional SIPMOS transistors and enhancing the supply voltages. Using the amplifier described here, output powers between 60 W and 160 W are obtained, figures which are not performance limits. Power supply uses two symmetrical supply voltages and needs no stabilization.

The drive circuit basically consists of two series-connected differential amplifier stages T_1, T_2 and T_{12}, T_{13}. As already mentioned, a dc and an ac negative feedback are obtained by an *RC* network between the inverting input of the first differential amplifier and the output of the output stage.

The operating point of the differential amplifier, T_1, T_2, is set by a current from transistor T_3 (current source). The collector current of T_5 determines the reference current of the current image. In order to protect the reference current from being changed by operating

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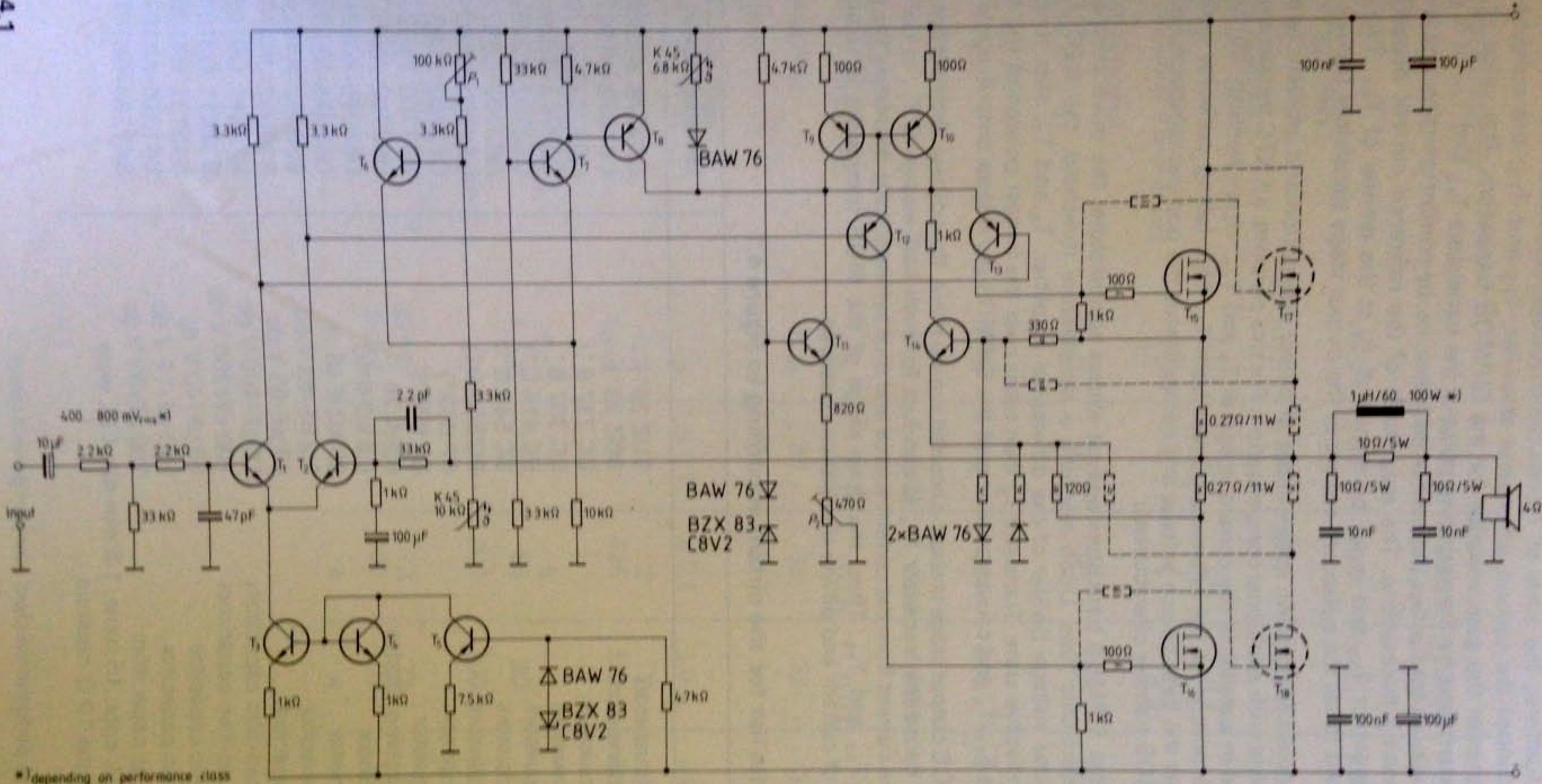
[1]) When connecting SIPMOS transistors in parallel, check whether the threshold values of the SIPMOS transistors used are approximately equal (measure!).

Figure 4.1


100 kΩ
P1
3.3kΩ
4.7kΩ
K 45
6.8 kΩ
BAW 76
4.7kΩ
100Ω
100Ω
100 nF
100 µF
T6
T7
T8
T9
T10
T12
1 kΩ
T13
100Ω
1 kΩ
330Ω
T15
T17
T11
T14
820Ω
0.27Ω/11W
1µH/60 100W *)
10Ω/5W
2.2 pF
3.3kΩ
400 800 mVrms*)
10µF
2.2kΩ
2.2kΩ
T1
T2
33kΩ
1kΩ
100 µF
K45
10 kΩ
P2
3.3kΩ
10kΩ
Input
33kΩ
47pF
BAW 76
BZX 83
C8V2
470Ω
P3
2×BAW 76
120Ω
0.27Ω/11W
10Ω/5W
10Ω/5W
4Ω
10nF
10nF
T3
T4
T5
1kΩ
1kΩ
7.5kΩ
BAW 76
BZX 83
C8V2
47kΩ
100Ω
T16
T18
1 kΩ
100nF
100µF
*) depending on performance class

voltage fluctuations, the base of T_5 has been voltage-stabilized. The output signals of T_1 and T_2 control the second differential amplifier, T_{12} and T_{13}, the collector currents of which generate the gate voltages for the SIPMOS transistors. The value of this gate voltage is determined by the operating point of the transistors T_{12} and T_{13}. It is generated in the same way as for the first differential amplifier, i.e. by current imaging and is stabilized against operating fluctuations. The magnitude of the reference current depends on the collector current of T_{10} and is set by means of P_2 at the emitter of T_{11}. The reference current is used to set the quiescent current of the output stage transistors (at $V_Q = 0$).

A constant quiescent current, independent of power dissipation and ambient temperature, is only possible with additional compensation. For this purpose, an NTC temperature sensor is connected in parallel to the current image of T_9 and T_{10}. Upon heating, the NTC takes over a small portion of the reference current from T_9. This falling collector current from T_{10} decreases the gate-source voltage and compensates the positive temperature response of the SIPMOS transfer characteristic.

To protect the SIPMOS transistors against excess temperature, the drive component includes an electronic fuse. Upon reaching a temperature threshold, the NTC thermistor in the T6 base voltage divider of the differential amplifier, T_6 and T_7, sets transistor T_7 into the conductive state. Transistor T_8 then takes over the largest portion of the reference current from T_{11}/T_9 and causes a limiting of the SIPMOS transistors output signal.

If the SIPMOS output stage is short-circuited during drive, the voltage drop across resistors $R_X = 0.27\ \Omega$ cause the transistor T_{14} to conduct for both half-waves. If T_{14} is conductive, it reduces the current from the current source and thus symmetrically decreases the collector currents of T_{12} and T_{13}. Thus, the drive range of the MOS transistors is reduced and a limitation of current and power dissipation is caused.

Components list for the circuit according to figure 4.1

Component		Ordering code
2 SIPMOS transistors	BUZ 20*)	C67078-A1302-A2
2 SIPMOS transistors	BUZ 23*)	C67078-A1002-A2
5 silicon transistors	BC 237 B*)	Q62702-C277
4 silicon transistors	BC 307 B*)	Q62702-C324
2 silicon transistors	BC 414 C*)	Q62702-C376-V2
2 silicon transistors	BC 546 B*)	Q62702-C687-V2
2 silicon transistors	BC 556 B*)	Q62702-C692-V2
1 silicon transistor	BF 869*)	Q62702-F592
1 silicon transistor	BF 870*)	Q62702-F602
5 silicon switching diodes	BAW 76	Q62702-A397
1 NTC thermistor	6.8 kΩ K 45	Q63045-K682-K
1 NTC thermistor	10 kΩ K 45	Q63045-K103-K
1 ceramic capacitor	2.2 pF/63 V dc	B38062-A6020-C206
1 ceramic capacitor	47 pF/63 V dc	B38062-J6470-G6
2 MKT stacked-film capacitors	10 nF/400 V dc	B32511-D6103-K
2 MKT stacked-film capacitors	100 nF/250 V dc	B32511-D3104-K
1 al electrolytic capacitor	10 µF/40 V dc	B45181-B4106-M
1 al electrolytic capacitor	100 µF/16 V dc	B41326-A4107-V
2 al electrolytic capacitors	100 µF/63 V dc	B41283-A8107-T
1 air coil 1 µH, appr. 15 turns, 1.5 mm dia. CuL wire wound upon the 10 Ω resistors		

*) depending on performance class (see component table)

Data sheet for the circuit according to figure 4.1

Output stage transistors		2× BUZ 20	2× BUZ 23	4× BUZ 20	4× BUZ 23	Unit
Supply voltage ($P_Q = P_{QR}$)	$V_S \geqq$	±33	±36	±40	±46	V
Supply voltage, max. ($P_Q = 0$)	$V_{S\,max} \leqq$	±38	±42	±50	±55	V
Current consumption						
($P_Q = 0$)	$I_S \geqq$	0.1	0.1	0.2	0.2	A
($P_Q = P_{QR}$)	$I_S =$	1.7	2	2.3	3	A
(short-circuit at the output)	$I_S \leqq$	1	1	1.8	1.5	A
Rated output power ($P_Q = P_{QR}$) ($f = 1$ kHz, $R_L = 4$)	$P_{QR} =$	60	80	120	160	W
Music output power ($V_S \leqq V_{S\,max.}$, $R_L = 4\ \Omega$)	$P_Q \leqq$	100	120	200	240	W
Harmonic distortion ($P_Q = P_{QR}$)	$k \leqq$	0.03	0.04	0.05	0.05	%
Intermodulation (250 Hz, 8 kHz, 4:1)	$m \leqq$	0.05	0.05	0.07	0.07	%
Input resistance	$R_I \leqq$	33	33	33	33	kΩ
Voltage gain	$G_V =$	31	31	31	31	dB
Frequency response (20 Hz...20 kHz)	$f \leqq$	±0.1	±0.1	±0.1	±0.1	dB
Transfer range ($4\ \Omega$, $P_Q = 0.1\ P_{QR}$)	$f_V \leqq$	2	2	2	2	Hz
	$f_{CD} \geqq$	450	425	300	250	kHz
Performance bandwidth ($k = 0.5\%$, $P_Q = 0.5\ P_{QR}$)	$f_V \leqq$	5	5	5	5	Hz
	$f_{CD} \geqq$	120	85	80	70	kHz
Attenuation ratio (4 Ω, 40 Hz)	$\geqq$	200	200	200	200	
Signal-to-noise ratio (CCIR)	$S/N \geqq$	73	73	73	73	dB
$P_Q = 50$ mW	$S/N \geqq$	104	105	107	108	dB
$P_Q = P_{QR}$						
Load resistance	$R_L =$	4	4	4	4	Ω

Transistors and resistors table for the circuit according to figure 4.1

Transistors	60 W	80 W	120 W	160 W
T_1, T_2	BC 414 C	BC 414 C	BC 546 B	BC 546 B
T_3, T_4	BC 237 B	BC 237 B	BC 546 B	BC 546 B
T_5	BC 307 B	BC 307 B	BC 556 B	BC 556 B
T_6, T_7	BC 237 B	BC 237 B	BC 546 B	BC 546 B
T_8, T_9, T_{10}	BC 307 B	BC 307 B	BC 307 B	BC 307 B
T_{11}	BC 237 B	BC 237 B	BC 546 B	BC 546 B
T_{12}, T_{13}	BC 556 B	BC 556 B	BF 870	BF 870
T_{14}	BC 546 B	BC 546 B	BF 869	BF 869
T_{15}, T_{16}	BUZ 20	BUZ 23	BUZ 20	BUZ 23
T_{17}, T_{18}			BUZ 20	BUZ 23

Resistors for short-circuit protection	a	b	c	d	x	y	
60/80 W	330	120	4,7 k*)	1,8 k*)	0,27	100	Ω
120/160 W	330	220	2,7 k*)	1 k*)	0,27	100	Ω

*) The operating point for the short-circuit protection is determined by these values and must be adapted individually.