THE CURRENT-MODE MUDDLE

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Abstract. With the arrival of monolithic processes for the fabrication of bipolar transistors during the mid-1960s, it seemed like a good time to examine new paradigms for design. Current-mode (CM) was attractive because it suggested that small voltages swings could be used to process analog signals represented as currents; whatever voltages that did arise were treated as *incidental*. These were good ideas at the time. Are they still true today? It is important to know when CM offers a real advantage, to know when it is truly valuable, and to know when it is of only passing and academic interest.

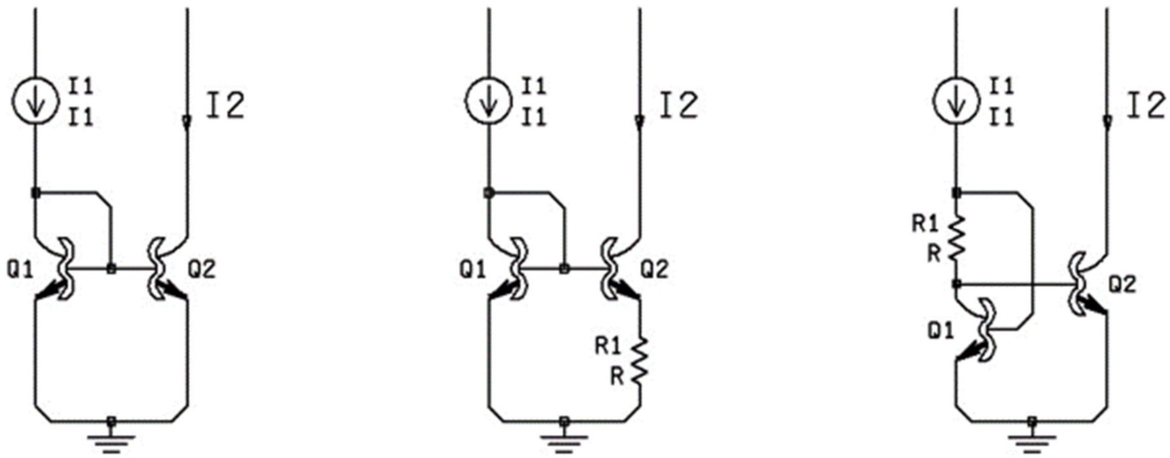
1 INTRODUCTION

The year is 1965, about a decade after the conception, by Jean Hoerni at Fairchild, of the planar process for monolithic transistor fabrication; and the year after I joined Tektronix to work on advanced oscilloscope design. The company was now ready to make monolithic circuits in its own dedicated wafer fab. We designers were hardly aware that a revolution in electronics was about to happen.

I was quickly swept up in all the exciting possibilities that monolithic integration afforded; many novel devices and circuits could now be invented and realized. For the first time ever, similar transistors *matched* very well, partly because of the accurate lithography and the fact that they operated at much the same junction temperature. This, in turn, allowed totally new kinds of circuit, compared with what we were used to in discrete form. And unlike vacuum tubes with their lethal supply voltages *{ a }*, transistors used safe, low voltages (often with collector-base voltages down even to zero – or even less!) and could handle currents from picoamps up to tens or even hundreds of milliamps.

It was inevitable that, during the coming years, the idea of processing signals exclusively in the current domain took hold. One of the new circuits that quickly gained attention was the ubiquitous current mirror *{ b }*, shown in its NPN implementation in **Figure 1a**. Here was a simple circuit that could not be realized with tubes, because they were 'depletion mode' devices: they conducted strongly even when their grid-cathode bias was zero. The bipolar junction transistor (BJT) differed in being an 'enhancement-mode' device: hardly any collector current, I_C, flows when the base-emitter voltage, V_{BE}, is zero. And more usefully, I_C increases in a precisely *exponential* fashion as this voltage is increased; this aspect was soon appreciated as the BJT's most potent characteristic. Further, a transistor's collector current can be readily *scaled* higher or lower simply by changing its size. These basic facts, which were apparent years before the arrival of CMOS, were to result in a long list of novel, intriguing and durable cells.

As shown, the input of the mirror is the current I_1 and its output is another current, I_2. Textbooks like to point out that $I_2 = I_1 \times A_2/A_1$ where the A's are the emitter areas. (Simple analyses assume that the two devices are isothermal, and overlook errors due to the base currents of both devices). But there is an important *voltage* hiding in this 'current-mode' circuit. It appears at the base node, and is generated by I_1 flowing in Q1. This voltage, which falls linearly with temperature (Sec. 2.1) is applied to the base-emitter junction of Q2; which, when isothermal with Q1, generates a scaled output current I_2. Realistically, a positive collector *voltage* at the output will significantly increase this current, due in part to the finite 'Early' voltage of Q2, and sometimes by its own power-induced self-heating. Setting these complications aside for the moment, we can regard this circuit as a 'pure CM' element, because *the input and output are both in current mode*.



(a) (b) (c)

Figure 1 (a) Basic Current Mirror (b) First Modification (c) Second Modification

But what about that *current source*, I_1? In the literature, it is assumed that one or more of these essential sources can be easily and accurately generated. In fact, they are often lost deep in the analyses, or are accurate only in ratio form. Sometimes, they are *dependent on other currents in the circuit*. They are usually precise only when incidental voltage effects in the CM cells are ignored. And while current sources are widely used for *biasing* purposes, in practice, the need for at least one *voltage* source – the 'supply' – always remains, because there is no way to generate a current without such. It is from such voltages that all of a circuit's currents are derived; which in turn means they are always at the mercy of *ohmic devices* for converting voltages to currents.

Now add a resistor, R, in the emitter branch of Q2 (**Figure 1b**). This simple modification is often used when a small current needs to be generated. It forces us to consider the *voltage* across this resistor, because it is *no longer incidental*. Clearly, I_2 will be lower than in the basic current mirror, all things remaining otherwise equal. It transpires that, even with ideal devices, there is no analytic solution for I_2. But when the *desired value for* I_2 is known, a solution for R immediately becomes tractable *{ c }*. Whilst this simple change is useful, we are already beginning to depart from a *pure CM concept*, in view of the fact that, even assuming I_1 is precise, *node voltages* now play an important role in its operation *{ d }*.

Moving the resistor from the emitter of Q2 to the collector branch of Q1 (**Figure 1c**) a simple analytic solution for I_2 is immediately straightforward, given the value of I_1, R and the emitter areas (which for now we will assume to be equal for the two transistors). With this modification, we can make an extremely tiny – nanoamps or less – output current from a substantial sourcing current. But we are now forced to abandon the idea of *pure CM operation*, because we are relying on the specific relationship between the collector *current* and the *voltage* V_{BE}. Before we can analyze this circuit, we need to better understand the BJT. Note in passing that little will be said about MOS realizations of these cells; but such is invariably quite straightforward.

1.1 The Ideal BJT Transistor

This paper is not intended to discuss subtleties of device physics and behavior, but rather, to reach a general conclusion as to whether there is any special value to CM operation. Accordingly, we will consider the use of the *ideal bipolar transistor* as it relates to the *development of topologies.* The ideal transistor *{ d }* is not limited by its forward current-gain (BF) or Early voltage (VAF); it has no parasitic resistances (RE, RB, RC) nor capacitances (CBE, CBC, CJS). We need to specify the bandgap voltage (EG) and the value of the saturation current (IS) at T = 300 K (it is an extremely strong function of temperature), and we include a finite base transit time (TF) simply to ensure that our circuits are well-behaved in dynamic simulations. Finally, to get $V_{BE}(T)$ closer to a more exact value, we must include the curvature term (XTI). Specific values are provided later.

With its emitter held at zero potential, and the collector-base voltage also close to zero, we apply a small positive voltage V_{BE} to the base terminal and note what happens to I_C. This is called the *normal active region* of operation. The basic relationship *{ e }* is stunningly simple:

$$I_C = I_S \exp\,(V_{BE}/V_K) \tag{1}$$

Note the symmetry: I_S is the *scaling current* for I_C while V_K is the *scaling voltage* for V_{BE}. (V_K is the *Kelvin voltage*, or thermal energy, kT/q, approximately 25.85 mV at T = 300 K). But the most notable thing about this expression is the *exponential relationship* of I_C to V_{BE}. This can be regarded as the heart of the BJT; and it has enormous practical value *{ f }.*

Why this digression into device theory, in a tutorial discussing the pros and cons of current-mode circuits? The answer (other than wishing to share the sheer beauty of that relationship) is that we find ourselves unavoidably face to face with the concept of *free-mode* design. The BJT is not, as often thought, a current-controlled current source; rather, it is a *voltage-controlled current source*; it is a *transconductance element,* g_m, like a vacuum tube of old (and in typical modes, like CMOS transistors).

Here's another pleasant surprise: by taking the derivative of I_C with respect to V_{BE} we find that the magnitude of the BJT g_m bears this relationship to the collector current:

$$g_m = I_C/V_K \tag{2}$$

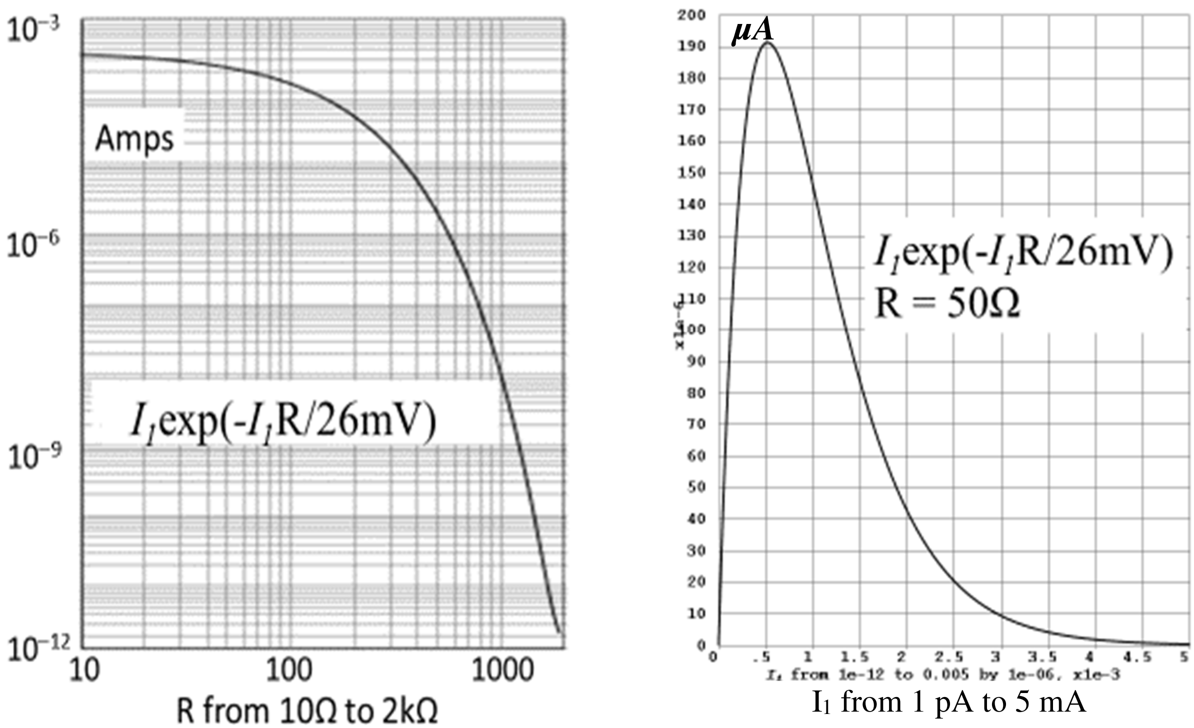
Again, we should surely be surprised by the pure simplicity of this statement. Here, even the scaling current I_S is absent. That's good, because it is a messy parameter whose value is minuscule (typically much less than femtoamps) at T = 300 K, and it varies by orders of magnitude over temperature *{ g }*. Most significantly, *the g_m is directly proportional to the collector current*, independent of the polarity of the transistor, its physical size, or even the material (germanium, silicon, silicon-germanium, gallium-arsenide, etc.) And we can optionally make this g_m temperature-independent by making I_C proportional to temperature; or, we can make variable-gain cells though controlling this current; and so on.

Eq. (1) can easily be reversed to yield V_{BE} given I_C:

$$V_{BE} = V_K \log\,(I_C/I_S) \tag{3}$$

Refreshed by this 'free-mode' outlook, *attributing equal importance to voltage and current*, we can return to the behavior of the current mirror of Figure 1c. As before, Q1 is obliged to operate at the supply current I_1; this sets V_{BE1} according to (3). However, the voltage applied to the base of Q2 is reduced by the voltage I_1R. So I_2 has the general form $xe^{-\alpha x}$:

$$I_2 \;=\; I_S \exp\left((V_{BE1} - I_1 R)/V_K\right) \;=\; I_1 \exp\left(- I_1 R/V_K\right) \qquad (4)$$



(a) (b)

Figure 2 The Output of the Fig. 1c Mirror, (a) versus R; (b) versus I_1

It is apparent that the output current of this cell can be made tiny for practical values of I_1 and R. Note that, at the unique value I_1R = V_K, the output attains its *peak value*: it exhibits a first derivative of zero and thus has no sensitivity *{ h }* to the drive current. When the emitter sizes of the transistors are equal (and thus $I_{S1} = I_{S2}$), the value of the output current is $I_1 \exp(-1)$ which makes I_2 about $0.368 \times I_1$. To restore the output current to this particular value of the input current, the emitter area of Q2 can easily by raised by the factor exp (1), about 2.718. The smallest integer ratio for unit emitters *{ i }* is 19/7 = 2.7143, resulting in a ratio error of under 0.15%. The overall accuracy of this cell depends as much on a careful consideration of voltages as of currents; but this is always the case in the practical design of every real circuit.

The same basic principles can be used in MOS circuits, with the benefit of near-zero gate current. But the mathematics is more complicated, even if it is assumed that the I_D to V_{GS} relationship is simply quadratic. (It rarely is, today, with the short channels in common use, and there are significant effects due to the drain and substrate voltages).

2 SOME EXAMPLES

It is by now clear that what is popularly called a 'current-mode' circuit may not fully justify the name. Consider the type of logic cell called 'current-mode logic' (CML). **Figure 3** shows a simple three-input OR gate. V_{REF} is the required reference, at the mid-point of the logic levels; Q5 is the level-shifting emitter-follower, which also provides power gain. Notice that *the inputs and the output are all voltages*. So a more accurate name for this type of cell is 'current-steering' logic. Indeed, the only currents are the tail I_T and the follower bias, I_O. These are not state variables but simple biases, just like numerous voltage-mode analog cells that use *non-critical* bias currents. A more complex structure, also imprecisely named a CML circuit, is shown in its BJT form in **Figure 4**; once again, all the logic inputs and outputs are *voltages*. Even when elaborated by the addition of active loads, or level-shifting followers, these cells remain firmly in the *free mode* class *{ j }*.

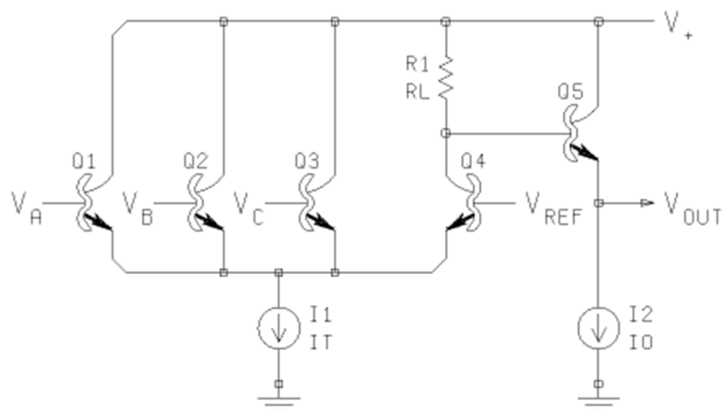


Figure 3 'Current-mode' Logic is really 'Voltage-Mode Current-steering' Logic

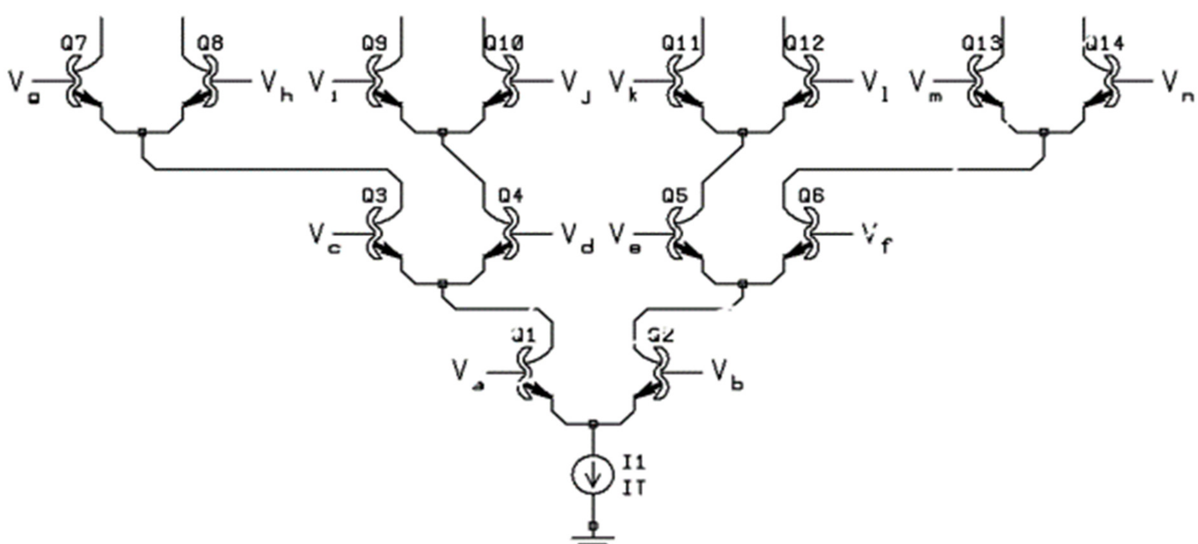


Figure 4 This Decoding Tree is also Incorrectly Called 'Current-mode' Logic

Another popular cell is the ‘current-conveyor’ (**Figure 5**). Ever since the invention of the original form (discussed later), the current-conveyor has become the darling of academia, and takes on several extended forms. The input can be either a pure current or, with little modification, it can be a voltage. Likewise, the output current may be used directly in a low-impedance load; but this current is often allowed to be converted to a voltage by the output impedance of the simple current mirrors *{ k }*. This voltage can be buffered by an output stage, as in the Current-Feedback Amplifier (CFA).

It is apparent that the signals – the *state variables* – can be in four alternative forms: (1) a current-input current-output source, (CCCS); (2) a current-input voltage output source (CCVS), in which case the scaling is arbitrary, because the effective resistance at the transimpedance node, TZ, is imprecise; (3) a voltage-input current-output source (a VCCS) with a reasonably exact transconductance, $g_m=1/R_{IN}$; or (4), as a voltage-controlled voltage output source (VCVS), again with imprecise, device-determined scaling.

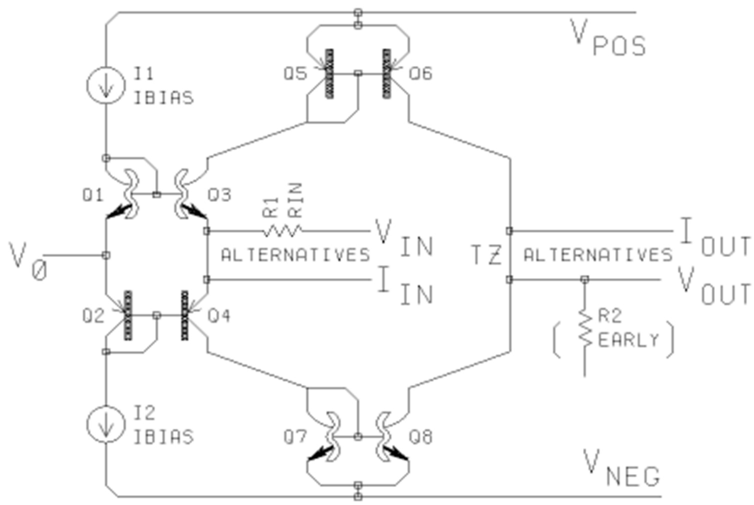


Figure 5 Various Arrangements of the ‘Current-Conveyer’ (see text)

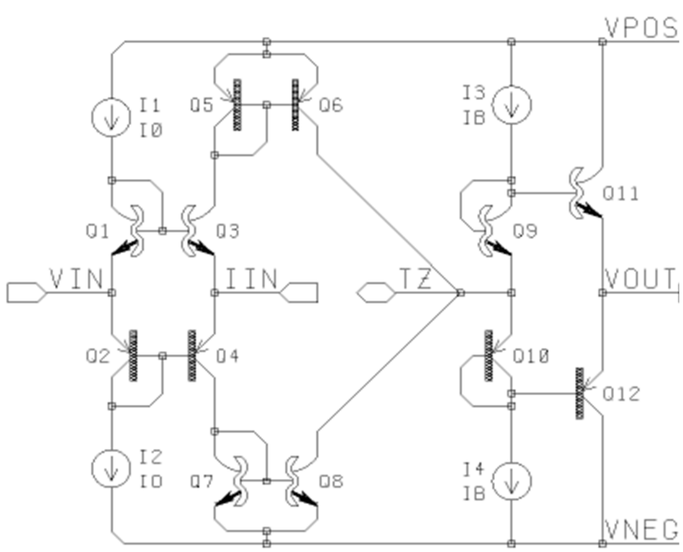


Figure 6 A CFA (Greatly Simplified AD844) uses a Current Conveyor

In the AD844 [1] the TZ node (**Figure 6**) is brought out to a package pin, to allow the external addition of a bandwidth-reducing capacitor, or simply when the function of a 'raw' current conveyor is needed (and the output stage is not used). Now, consider the *linearity* of this *open-loop* function. Using a bias of I_0 it is easily shown *{ l }* that in response to a *normalized input current,* σI_0, applied *toward* the current-mode input, the collector currents in Q3 and Q4 are *nonlinear*:

$$I_{C3} = I_0\,(\sqrt{(\sigma^2 + 4)} - \sigma)/2 \quad \text{and} \quad I_{C4} = I_0\,(\sqrt{(\sigma^2 + 4)} + \sigma)/2 \qquad (5)$$

These two currents (**Figure 7a**) recombine to form a linear output *provided that* the scaling of the two current-mirrors Q4-Q5 and Q6-Q7 is precisely equal. The residual open-loop nonlinearity for a mismatch of 5% in one of the mirrors is depicted in **Figure 7b**. These plots are for an input current of up to 2σ (here, ±200 µA). For large inputs, one or the other halves of the current conveyor dominates and the open-loop response tends toward linear.

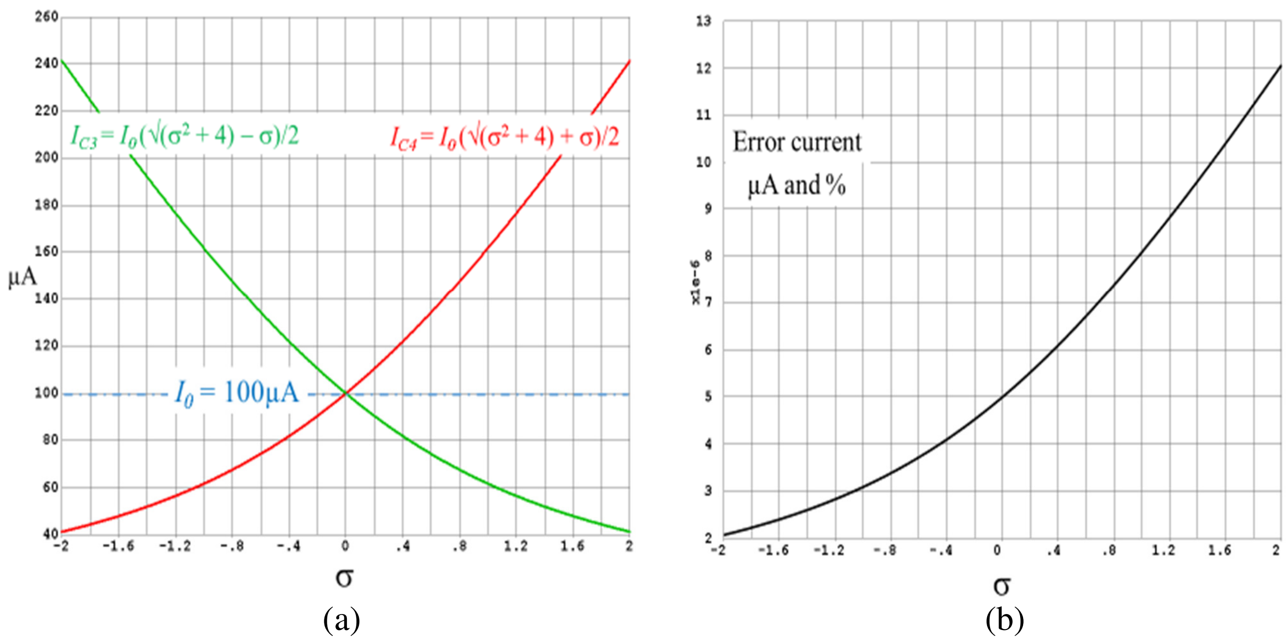


Figure 7 (a) A Current Conveyor is Inherently Nonlinear (b) The Output Error for a 5% Mirror Mismatch

In the current-feedback amplifier, the *closed-loop* gain is little affected by the value of R_{TZ}. In the usual case (where the buffer has a gain of unity) this resistance is effectively in simple parallel with the feedback resistor, R_F. Thus, under closed-loop conditions, the output is $V_{OUT} = I_{IN}\,(R_F // R_{TZ})$. When an R_F of typically1 kΩ is used, the shunting effect of R_{TZ} – typically many megohms – is negligible, and in practice has exactly the same effect on gain as a simple error in the absolute value of R_F. For similar reasons, the open-loop distortion described by Eq. 5 is almost totally suppressed in closed-loop operation of a CFA.

When the net capacitance, C_{TZ}, is included in the impedance of the TZ, an *open-loop* pole at $R_{TZ}C_{TZ}$ is formed, while under closed-loop and lightly-loaded conditions the pole is at the much higher frequency, $R_F C_{TZ}$. The high slew-rate of a CFA results from the large-signal error current into the TZ node. This is very different from the typical voltage-mode op amp, where the slew-rate is limited by the tail current of a differential input pair.

2.1 Simplifying Simulation Studies

It was noted that the simulation of analog cells is better pursued, at least initially, using *highly idealized transistors*, to determine the general 'shape' of some function. This is not so very different from the manner in which textbooks present an 'analysis' of a circuit *{ m }*. A key advantage of ideal models is that they are *portable* from one simulation platform to another, where they produce identical results (provided such factors as the convergence tolerances are maintained). The results also are free from the often vexing complexities incurred by the use of detailed models *{ n }*. These are the parameters used to examine the general behavior of the circuits discussed in this paper:

BF=1E6; BR=10; VAF=1E6; VAR=10; XTI=3; EG=1.145; IS=2.51E-17; TF=1p

The 'ridiculously high' values for BF and VAF avoid errors arising from base current or collector voltage; while if RE, RB, RC, CBE, CBC and CJS are left undefined they automatically default to zero. EG and XTI are required in voltage reference design. A finite TF avoids oscillations due to unwanted HF effects. The parameters of the 'Ideal PNP' are identical; the departures from exact complementarity are later absorbed in the higher 'Levels' layers (see endnotes) and will generally *not* be the same for the two polarity types. Recall Eq. (1):

$$I_C = I_S \exp(V_{BE}/V_K) \tag{1}$$

Using the T = 300 K values of $I_S = 2.51\text{E-}17$ and $V_K = 25.85$ mV, we find that for an *applied* V_{BE} of **750 mV** we have

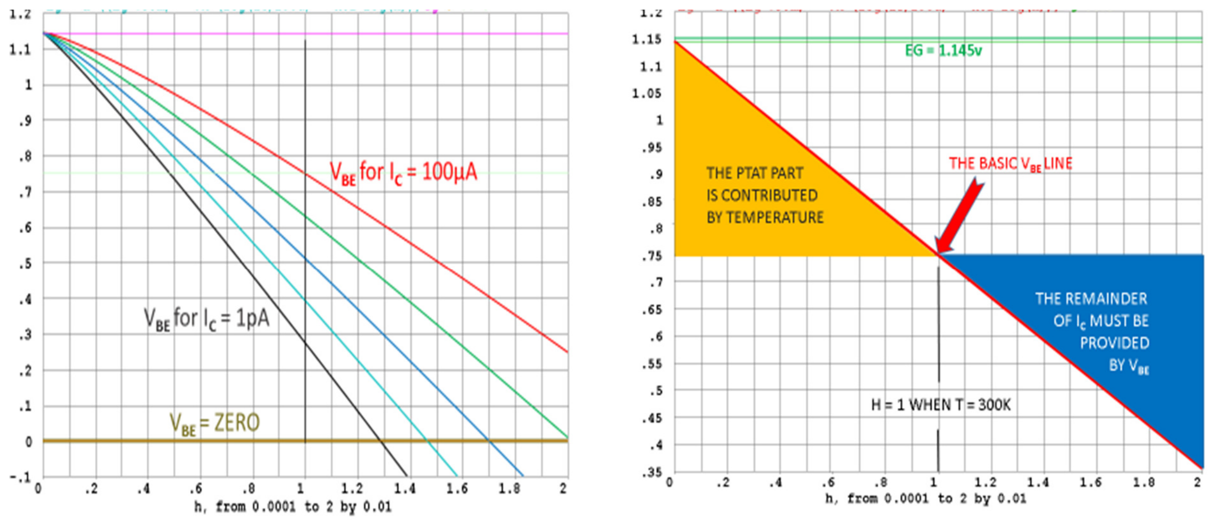
$$I_C = 2.51\times10^{-17} \times \exp(750/25.85) = \mathbf{100\ \mu A} \tag{6}$$

These benchmark values for V_{BE} and I_C stem directly from the value of I_S. Eqs. (1) and (3) are useful in the general design of current-mode circuits. A more complete and practical expression for V_{BE} as a function of I_C is given below. Note that, now, V_{BE} is *firmly rooted in EG*, and varies with H = T/T$_N$, where T$_N$ is a 'normalizing temperature' (often 300 K). This equation completely avoids the use of I_S, which is too small for direct measurement, while V_{BEN} (the V_{BE} at T = T$_N$) and $I_C = I_{CN}$ are easily measured in practice.

$$V_{BE} = \mathrm{EG} - \mathrm{H}\left[(\mathrm{EG} - \mathrm{V_{BEN}}) - \mathrm{H}.V_K \log(I_C/I_{CN}) + V_K.\mathrm{XTI}.\mathrm{H}\log\mathrm{H}\right] \tag{7}$$

Hence, at H = 0 (absolute zero), V_{BE} would need to be fully equal to EG (here, 1.145 V) for *any conduction* to occur. **Figure 8a** shows how V_{BE} ideally varies for a range of I_C values from 1 pA to 100 µA in steps of ×1000, using Eq. 7 with XTI = 3. Note also that the voltage (EG – $\mathrm{V_{BEN}}$) is a constant for any given device (that is, for a given I_S at H=1).

The realization that V_{BE} can actually be zero (or even negative), and the explanation of why it declines almost exactly in a linear way (based on simple fundamental considerations) are aspects of the BJT that, to my best knowledge, have never before been published; which is surprising in view of the many years that BJTs have been used.



(a) (b)

Figure 8 V_{BE} as a function of H = T/T$_N$ (a) with XTI=3 (b) with XTI=0 and explanation

So let us reconsider these important aspects of the V_{BE}. First, at very low currents and high temperature, V_{BE} falls to zero; it can even become *negative!* (This is a verified fact in ICs designed for the measurement of extremely small currents). Then, an XTI of 3 (it is larger in practice) causes little curvature over the range T = –55ºC (that is, H = 0.727) to T =125ºC (H = 1.33). The curvature factor H log H appears in many advanced analyses of BJT circuits, and needs to be considered. Remember also that at T = 300 K the V_{BE} increases by nearly 60 mV for each decade increase in I_C – a voltage which, of course, is basically PTAT.

Setting XTI = 0 (**Figure 8b**) we see that V_{BE} decreases *exactly linearly* with temperature. It has to be that simple, because both voltage and temperature are proportional aspects of *energy*. Thus, the energy donated to the junction by temperature increases as shown by the orange triangle – it is *proportional to absolute temperature* denoted as PTAT. The rest of the energy must be supplied by the *voltage* applied to the base-emitter junction, the V_{BE}, which voltage we speak of as having overall a CTAT form *{ o }.*

So finally, we can define what constitutes a *pure current-mode* cell. The principle requirements for such a cell are:

1) Signals to be generated or processed are represented by currents; that is, all the *state variables* are in the form of currents.
2) All current-input nodes should desirably present a low impedance.
3) All current-output nodes should desirably present a high-impedance.
4) Biasing of pure-CM cells takes the form of currents, sometimes derived from signal currents elsewhere in the complete circuit. The bias currents must usually be arranged in *ratioing pairs*.
5) Pure CM cells should exhibit *accurate scaling* of input/output ratios, independent of process variations, temperature, etc. (the PVT criteria).
6) *No inertial elements* can be added to a CM circuit; but allowance is made for those inherently due to the active elements, or as needed for 'HF compensation'.

The last criterion excludes circuits in which the state variables are of the *time* dimension. So it is technically incorrect to speak of a 'current-mode oscillator' or a 'current-mode filter', because any circuit in which time plays a key role must include some form of *energy storage*, such as one or more capacitors, inductors, transformers, delay-lines, etc. A review of the extant CM literature shows that this requirement is often overlooked [2, 3]. However, much depends on the particular objective of the circuit. Thus, with some relaxing of this criterion, it is permissible to regard 'log-domain' filters (translinear filters) as CM circuits, or such things as RMS-DC converters; in either case at least one capacitor is essential.

3 EARLY CM WORK

The mid-1960s at Tektronix saw an increasing confidence in monolithic BJT processes and led to the invention (or perhaps it was the discovery?) of numerous cells that depended either directly or indirectly on the unique properties of the BJT, where the pivotal idea was to *use currents as signals*, rather than voltages. Here's some of that history.

Early on, I wondered whether one might design a *current-mode dual* of the high-gain IC 'op amp' – a VM device – then gaining popularity. To be a formal dual, the inverting and non-inverting inputs should accept input currents at low-impedance nodes and the output should be a current delivered from a high-impedance node. Clearly, such an IC would need a special sort of current mirror that could accept a *bipolarity input*, using the dual supplies available in many systems of the time. This implied the use of *complementary* and *well-balanced* PNP and NPN devices. But at that time, the only PNP transistors available were lateral devices having very low current gain and poor dynamics. Still, I thought they might work well enough to prove the idea; and as it turned out, they had some unforeseen merits.

It became too complicated to arrange for *both* input nodes to have identical characteristics; but it was easy to devise a cell in which *one input was a current and one was a voltage*, while the output was in current form. Because this new cell conveyed a *bipolarity* input current to a *bipolarity* output, I named it a *Current Conveyor,* to clearly distinguish it from the simpler unipolar current mirror. This term quickly spread by word of mouth within the Tek labs, and was suggested at various meetings and conferences; but no JSCC paper or patent was ever written. Back then, the focus was on *creating*, rather than *protecting*, ideas. Consequently, very few patents on simple, basic cells were filed. Anyway, it seemed like too trivial a topology to make a lot of fuss over: in essence it was just a 'mirrored mirror'.

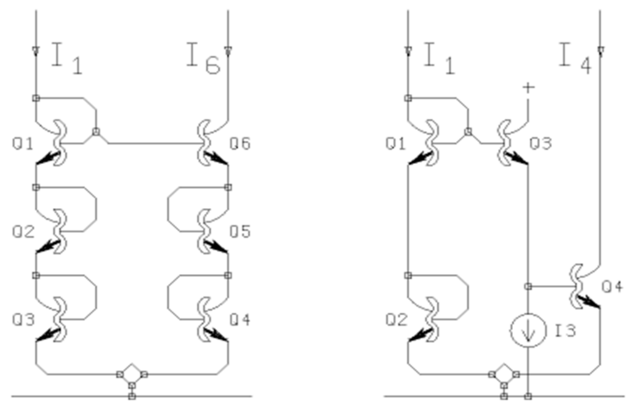
The voltage applied to the relatively high-impedance voltage node was replicated with near-unity gain, within millivolts, at the current-accepting input. In a current conveyor, its unloaded output voltage can rapidly swing almost rail to rail, offering a high 'voltage gain'. This suggested that it would be of more practical value to just buffer this voltage, rather than stubbornly retaining the earlier objective of providing a current output. That's how the first CFAs were realized, using lateral PNPs. In later years, at Analog Devices, my specifications for a *fully-complementary* IC process were eventually heeded. A practical CFA *product* could finally be mass-produced. This product, the AD844, achieves a slew-rate of 2,000V/μs, rarely equaled even on today's high-speed processes; and it provides a fast, overshoot-free pulse response. It is still competitive. This product is highlighted here because it clearly exemplifies what is called *'free-mode'*. It starts with a current conveyer – not quite a pure current-mode cell – and ends with a simple voltage-mode buffer.

3.1 Translinear Circuits

While at Tektronix, I wasn't yet fully satisfied with mixed-mode circuits, such as the CFA. I still wanted to make circuits that could reap the potential advantages offered by *pure current-mode* operation, chief being that signals could be supported by very small voltage swings. For example, a change in V_{BE} of only $\pm V_K$ (about ±26 mV at 300 K) results in a change in I_C by a factor of almost 7.4 (e^2), enough to unambiguously represent a signal. The low impedance nodes associated with these small voltage swings promised that circuit capacitances should have only a small effect on the dynamics of the circuit. Starting in this way, it quickly became apparent that endless, practically-useful circuits could be devised by the use of *extended loops of exponential junctions*. The basic current mirror – the simplest translinear circuit – has just one such loop, containing two junction devices.

Consider the effect of stacking junctions as shown in **Figure 9a**. There are three in both the input and output leg of this extended current mirror. Assigning the emitter areas as A_1 through A_6, respectively, we can immediately write – without any math to speak of – that

$$I_6 = I_1 \times A_6A_5A_4/A_3A_2A_1 \qquad (8)$$



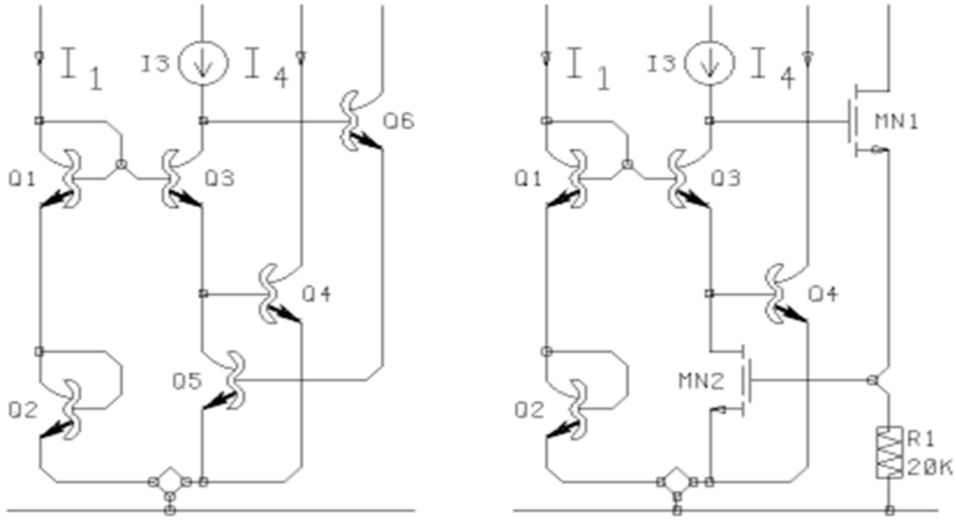
(a) (b)

Figure 9 (a) Extension of the Current Mirror (b) a More Useful Arrangement of Just Four Transistors

But this isn't of much practical use, even if we are trying to make a mirror that linearly increases or decreases an input current by some considerable factor. There are better, more economical ways of achieving such a simple operation. Consider, for example, the four-transistor cell shown in **Figure 9b**. Using what we have already learned (and still assuming ideal transistors) we can easily see that the function is now

$$I_4 = I_1^2/I_3 \times A_4A_3/A_2A_1 \qquad (9)$$

So now we have *a pure current-mode squaring cell*. This is already looking more useful. You can probably see what has to be done to this arrangement of devices to realize a *square-rooting* cell or a rudimentary *one-quadrant multiplier*. The door has been opened! Thinking more practically we might first address the base-current errors when using real transistors. A *tail-chaser* can be valuable, as shown in **Figure 10a**. The multiplied current gain of the cascaded NPNs is high, making the I_C of Q3 is essentially equal to I_3. A better arrangement in a modern BiCMOS process would replace Q5 and Q7 with NMOS devices, as shown in **Figure 10b**, ensuring an even more exact replication of I_O in Q3.



(a) (b)

Figure 10 (a) A Simple CM Multiplier (b) an Improvement Using a BiCMOS Process

The ideas are leaping off the page! So now, we need to be just a little more formal. Let's summarize the general form of a translinear circuit; there are 2N junctions in a ring, and

1) Summing the exponential junction voltages in the clockwise (CW) direction, that is, for $1 < n < N$, they are each of the form $V_K \exp(I_n/A_n I_S)$; these are equated to the voltages in the CCW direction, numbering $(N+1) < n < 2N$, also exponentials.
2) The algebraic sum of these exponential voltages must be zero around the loop.
3) Assuming the cell is isothermal, the voltage V_K and the saturation current, I_S are the same for all devices, and they cancel on the CW and CCW sides of the equation.
4) Finally, expressing the junction currents in their *current-density* form, $J_n = I_n/A_n$ we can state the most concise form of the translinear principle:

$$\prod_{n=1}^{n=N} J_n \equiv \prod_{n=N+1}^{n=2N} J_n \tag{10}$$

This is the foundation of a large class current-mode circuits, that is, the *pure current-mode* cells called *Translinear Circuits*. By the late 1960's there were dozens of cell topologies of this class, providing numerous linear and nonlinear functions. But in the absence of a generalized formulation, these cells were known by many different names *{ p }*. It is worth mentioning that simulation played no significant part of exploring these early cells: powerful new insights were gained from pencil-and-paper doodling alone, and by insistently invoking that most important question for the curious, inventive mind: *What If?*

Eventually, I proposed a formal name, in a 1976 note in Electronic Letters now largely forgotten. This became the basis of several PhD theses, one of which was written under my guidance as thesis advisor to Evert Seevinck; we identified twenty-six unique translinear cells having describing equations up to 4^{th}-order. He later published this thesis as a book.

3.2 More Examples

To further illustrate the potency of translinear (TL) design, we will first consider its use in a variable-gain wideband amplifier. **Figure 11** shows a simple gain cell; assume for now that all the transistors are identical. The signals are applied as a complementary { q } pair, $(1+x)I_X$ and $(1-x)I_X$, where $-1 > x > +1$. These set up an (incidental) input voltage across the emitters of Q1 and Q2:

$$V_{IN} = V_K \log \frac{(1+x)}{(1-x)} \qquad (11)$$

Notice that not only does the basic I_S not appear in this translinear analysis, but here, neither does the bias current, I_X. The *modulation factor*, x, results in a differential input voltage (at the emitters Q1 and Q2) of ±76 mV at T = 300 K for a peak signal input of $x = 0.9$.

At this point, we can either continue our analysis in 'voltage mode', or we can greatly simplify the analysis by considering the translinear loop formed by the four transistors, and simply writing the translinear equation for the relationship between the input x and the variable y. The bias currents I_X and I_Y will not appear in the equation, because they appear in cancelling pairs. So we are left with

$$(1+x)(1-y) \equiv (1-x)(1+y) \qquad (12)$$

This means that the internal state variables x and y are simply equal. Summing the output currents of Q3 and Q4 with the replicated input currents at the collectors of Q1 and Q2, we find that the *pure current-mode gain* of this cell is simply $1 + I_Y/I_X$.

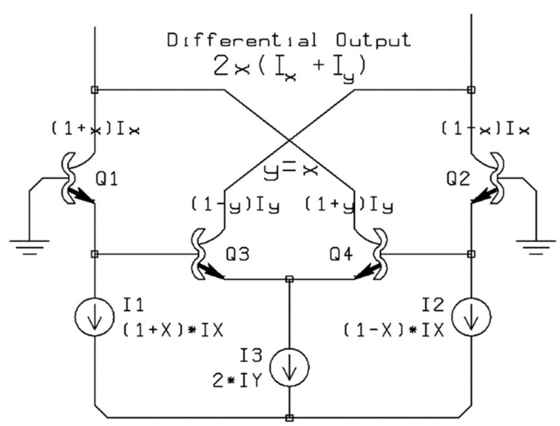


Figure 11 Example of a Simple Variable-Gain Amplifier

The same sort of translinear potency is illustrated in **Figure 12**. This simple CM circuit accepts input currents $+I_X$ and $+I_Y$ and generates an output that is their *one-quadrant vector sum* $\sqrt{(I_X^2 + I_Y^2)}$. The circuit may be extended to accept any number of inputs by simply adding input branches and increasing the number of *partial* outputs, all sharing the transistor QZ; or to compute successively higher-order roots by increasing the number of transistors in each input branch and adding series-connected QZ transistors. Thus, it is an easy matter to compute such terms as $\sqrt{(I_X^2 + I_Y^2 + I_W^2)}$, or $(I_X^4 + I_Y^4 + I_W^4)^{1/4}$, and so on.

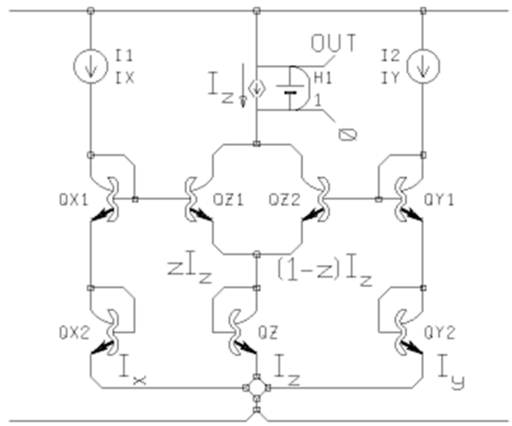


Figure 12 A Two-Input Vector Summer

The reader is left to devise and analyze these high-order extensions, but to help a little, the following explanation of the Figure 12 cell is provided. The current I_Z is unknown at the outset, except that we know it must eventually flow in QZ; thus, we can divide it into the two components zI_Z and $(1\text{-}z)I_Z$. That leads to the pair of simultaneous equations

$$I_X^2 = zI_Z^2$$
$$I_Y^2 = (1-z)I_Z^2$$
$$\text{Thus:}\quad I_X^2 + I_Y^2 = I_Z^2. \qquad \text{QED}$$

As a further exercise, try to adapt this form to more usefully accept *bipolarity* inputs. Hint: look again at the topology of the current conveyor.

4 DISCUSSION

The debate over the quest for an optimal choice for an analog system's state variables – that is, whether it is better to emphasize voltage or current– rages on in academia, over fifty years since it first arose. It is still pondered by many IC designers around the world. The part of this population who are *professionals in the business of developing products* to serve the world marketplace are unaffected by this debate; they instinctively use whatever signal modes make the better choice, which usually vary from one cell design to the next. These designers have little time to write arcane papers about rudimentary cells; they are often too busy to digest even the content of professional journals. They tend to insulate themselves from the background noise and focus on their current assignment.

The remainder – teachers, bravely constructing curricula that are thought to be the most appropriate for the times, or students seeking to pursue a theme that might yet provide hidden benefits – still feel there is something to be gained by embracing the current-mode view of design. They produce by far the largest volume of papers and in so doing, they influence the thinking of others pursuing similar goals. Their knowledge of the history of electronics is often limited to the past few years, as are the references they append. It is essential to be aware of future changes that will affect one's decisions, such as the opportunities afforded by new devices, materials and technologies, but it is a mistake to take the position that ideas from the deep history of electronics are of little value today.

Long before the monolithic era, it was fashionable to suppose that the use of current-mode cells *{ r }* must, surely, have some advantages in modern electronic circuit design. There certainly seemed to be a lot of people talking about current mode this or that. During the 1980's, university courses eventually appeared followed, which taught (and in some cases seriously over-emphasized) current-mode design principles. Since then, the professional journals have devoted entire issues to share CM ideas; and conference sessions have been convened to discuss perceived advances between committed advocates of this approach.

It is notable that, among the dozens of papers that extol these special virtues, few if any spend little time explaining *why* the CM paradigm should be *inherently better* than any other. As noted, their references point mostly to very recent papers, some often less than a year old, in which a student designer has adopted the CM approach to cell design believing that its *sheer novelty* assures its intrinsic value, which until now has been 'neglected'.

We have to ask ourselves: can we point to any *compelling*, and, in the most favorable cases, *truly unique*, advantages? Are CM cells of *general* value, capable of everyday utility? Or are they merely fashionable? The justification to use CM methods may simply be founded on the fact that modern ICs operate from small supply voltages. In such cases, 'pure CM' might be better suited to the contemporary reality. But then, they actually belong to the category of low-voltage (LV) design. This class has become important for at least two good reasons: (1) the increasing use of CMOS and BiCMOS processes that emphasize operating speed and packing density, having low-voltage characteristics; (2) the present-day drive to achieve more mixed-mode functions with ever less power. These factors may, or may not, suggest an advantage in processing signals in the pure current-mode; consequently, it does not automatically follow that 'pure CM' is better suited to today's real-life demands. There are times when the use of *neither* voltage mode nor current mode is optimal. For example, *charge-mode* is the first choice in modern data converters and for switched-capacitor filters; *frequency-mode* or *phase-mode* signals are often used in communication systems.

My own experience in IC product development has required the full embrace of what I refer to as the *Free Mode* perspective [5]. It is essentially a call for vigilance, rather than another design dogma. It is simply *a way of thinking* – before settling on an optimal approach – about how best to deal with a practical design challenge. It exercises the mental muscles that allow one to leap, *quickly and with instinctive ease*, from one mode of signal representation to another.

Finally, it is very important to be ever aware of the *layout* of a new circuit or product, well before completing the (frequently, strongly schematic-anchored) design *{ s }*. In this respect, remember that even the most capable simulators can be misleading unless one includes all the many incidental and subtle resistances, capacitances and inductances of the emergent layout. This requires comprehensive *post-layout back-annotation*. In microwave practice, it is frequently essential to use electromagnetic modeling of critical aspects of the layout, and of the package, to more fully account for all the parasitic elements and effects encountered in the ultimate user's final board layout.

5 CONCLUSION

For decades, electronic signals have been generally represented as voltages. This can be attributed, at least in part, to Lee de Forest's invention of the triode vacuum tube. In a typical amplifier, its grid voltage, with near-zero grid current, would modulate the current flowing from cathode to anode. This was immediately converted back to voltage mode by the anode load impedance in shunt with the triode's internal output resistance, providing a modest voltage-mode (VM) gain. In this case, the tube's current is an *incidental variable*.

But the persistence of the VM view in recent times also has practical justifications. For example, voltage nodes can be probed by instruments, and accurately measured without breaking circuit branches. Thus, in CMOS logic the state of a system can be determined using the roving single-sided probe of an oscilloscope or logic analyzer. And at moderate frequencies, the VM gate outputs can drive other gates without much concern about loading. Even when hiding behind a moderate impedance, any type of cell output can drive other voltage-mode circuits and can be probed with only a small effect on measurements. Such benefits pose obvious advantages in both analog and digital practice.

Of course, the 'VM view' is itself just another convenient simplification. Transient *current* must flow at the input of a logic cell to alter the *charge* on the gate oxide, and thus the channel *current*; and the delay and transition times are affected by loading capacitance, particularly in the longer connections between gates. However, these currents are not signals; they are an unavoidable – an *incidental* – aspect of circuit operation. Nonetheless, a thorough design requires consideration of how these current-mode aspects are addressed. A CM cell may often be translated to its VM dual, one being *more practical* than the other.

In many IC's the state variables may be fully defined by *system charges*, but there is an obvious practical snag here. At the interfaces of charge-mode (QM) circuits, the input and output signals will eventually have to be represented as voltages or currents. QM cells cannot speak directly to a typical 'board level"; they must usually undergo a suitable translation both entering and exiting the boundary of a cell. The practical appeal of QM is that miniscule (but fragile) amounts of charge can be used as state variables.

If, after all, CM realization of a function still seems to be preferable, even with significant alterations to a circuit's topology and the use of current-mode interfaces and current-source biasing, then it might be time to consider it. The fact remains that, before proposing yet another 'current-mode something', it is important to carefully consider all the relevant factors. It's never too late to realize that what one's CM approach is has no inherent merit after all. Often, it is nothing more than just *another way* some function can be realized.

There is no inherent guarantee, *nor should there be*, that any one of numerous signal processing modes offers a clear and compelling advantage over some other. The choice is invariably a pragmatic one, based on issues of convenience; or the availability of known and trusted cell concepts which can quickly be adapted; or the natural and comfortable fit of the cell within a product framework. Beyond the small-circuit boundary, and often even within it, the representation mode will generally change fluidly and frequently. Thus, we can say with full assurance that the design of circuit cells always requires the sure-footed application of the *Free Mode* viewpoint [5].

END-NOTES

{ *a* } The two-tube Philbrick op amps used supplies of +/–300 V and consumed 7.4 Watts, mostly in the tube filaments.

{ *b* } Interestingly, tracing the invention of this simple circuit has not found the source. It probably happened at Fairchild soon after their first monolithic process. The author has confirmed that it was neither Dave Fullagar nor Bob Widlar.

{ *c* } This is because the describing equation is transcendental; that is, I_2 is equal to a logarithmic term in which I_2 appears again. This simple ruse of reversing Cause and Effect is of great value in numerous cases where the 'forward' analysis hits the transcendental barrier.

{ *d* } Using the standard SPICE names for these basic parameters; of course, we will eventually need to be much more detailed.

{ *e* } Very slightly simplified. At extremely low currents (where $V_{BE} \approx V_K$) and operating at high temperatures it will be $I_C = I_S (\exp(V_{BE} / V_K) - 1)$.

{ *f* } William Shockley spent a lifetime considering the complexity of semiconductors materials. That the behavior of the BJT boils down to something so fundamental can only be called remarkable.

{ *g* } If we wish to be sentimental, we might think of I_S as the BJT's 'soul'.

{ *h* } In practice, we can only say that the sensitivity of I_{C2} to I_{C1} is at or near a minimum.

{ *i* } For now, we will avoid the debate as to which is 'more fundamental': a voltage or a current.

{ *j* } Ratioing using integer numbers of unit elements is an essential aspect of all robust designs.

{ *k* } For this reason, the mirrors are often of the Wilson type with emitter resistors added to improve the ratio accuracy and reduce the noise contribution of the mirrors. The complete optimization of a CFA has to consider many such issues.

{ *l* } Using the simple rules of translinear circuits; see Sec. 3.1.

{ *m* } Even the dominant pole of the poorly-defined generic op amps, used in text-book studies of frequency-dependent circuits, is completely overlooked; the amplifier is treated as if an ideal element having infinite gain and zero output impedance at all frequencies. In fact, a more appropriate simplification of the function an op amp is that of a pure integrator, whose unloaded output is $V_{OUT}=(\omega_o/\omega)V_{IN}$ where ω_o is the frequency at which the gain drops to 0 dB, that is, to a voltage gain of unity, and ω is the frequency of the signal of interest.

{ *n* } This is the first step in *'Foundation Design'*, which is the formal approach to deep under-tanding and the generation of valuable insights in a step-by-step way. In that philosophy, the use of ideal elements is called a 'Level 0' analysis. Then, one adds an increasing amount of realism in the higher-numbered Levels, finally using the most complex models, for 'almost real' simulations.

{ *o* } The term PTAT was proposed by the author in a 1976 JSCC paper and is now widely understood. Less well-known is the manner in which V_{BE} is complementary to absolute temperature, prompting Paul Brokaw to add the term CTAT.

{ p } One of the first names for these cells was 'MAGIC' – an abbreviation for '*Monolithic Amplifiers for Gain Control*'. The later word 'translinear' (1976) suggests the realization of accurate linear functions using severely nonlinear elements.

{ q } *Complementary* pair of signals differs from a simple *differential* pair of signals. In the example considered, the two input currents always sum to I_X. But in a differential input, we have the uncertain additive effect of a common mode current, I_{CM}.

{ r } A cell is defined as any small ensemble (up to, say, about a dozen) elements having a defined design objective.

{ s } It is assumed that one's real circuit designs are not directed by some set of equations, which usually are simplified idealizations.

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